An ultra-low noise fully-differential amplifier

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Abstract

A general-purpose instrumentation amplifier must be dc-coupled and have a differential input to handle both differential and single-ended input signals. It also must exhibit low input noise in both voltage and current, to accommodate a wide range of signal source impedances. Additionally, having a differential output is desirable to allow direct connection to current high-resolution analog-to-digital converters (ADCs) which have differential inputs. There are commercially available devices with \( e_{n} \) voltage noise spectral densities as low as 1 nV/\( \sqrt{\text{Hz}} \) but present high \( e_{n} \) current noise spectral densities \( i_{n} \) of a few pA/\( \sqrt{\text{Hz}} \). On the other hand, there are also devices with \( i_{n} \) as low as a few fA/\( \sqrt{\text{Hz}} \) but presenting \( e_{n} \) around 10 nV/\( \sqrt{\text{Hz}} \). To obtain low values of both \( e_{n} \) and \( i_{n} \), a fully differential circuit topology combining discrete Junction Field Transistors (JFET) and Operational Amplifiers (OA) is proposed. Design equations, stability analysis, and experimental results are presented. As an example, a fully differential instrumentation amplifier has been designed, built, and tested showing \( e_{n} < 1 \) nV/\( \sqrt{\text{Hz}} \) @1 kHz and \( i_{n} < 10 \) fA/\( \sqrt{\text{Hz}} \) @1 kHz. The proposed topology finds applications such as front ends for measuring and testing instruments, industrial instrumentation, and audio circuits.
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Index Terms — low-noise amplifiers, fully-differential circuits, instrumentation amplifiers.

I. INTRODUCTION

Low impedance sensors such as strain gauge bridges, magnetometers, moving coil phonograph cartridges, microphones, and geophones among others, feature very low source impedances, of a few hundred ohms and lower. Their intrinsic noise is very low, thus demanding instrumentation amplifiers with voltage noise spectral densities below $1 \text{nV/}\sqrt{\text{Hz}}$ to avoid degrading the sensor signal-to-noise ratio (SNR). This kind of devices, denoted as ultra-low noise amplifiers, are difficult to implement with commercially available integrated circuits and must be solved by hybrid amplifiers, which combine operational amplifiers with discrete transistors in the input stage [1], [2], [3].

The lowest noise level is achieved with single-ended hybrid amplifiers since they can be designed to present the noise of a single active device [1], [4]. However, the use of this kind of amplifier is limited to sensors with single-ended output and requires very low-noise supply and bias voltages [4], thus restricting their use in those laboratory applications. On the other hand, the input-referred noise of a differential amplifier topology corresponds to the contribution of the two transistors composing its input stage. This is a bit higher than the single-ended case, but power supply and bias voltage noises work as common-mode sources and do not contribute significantly to the overall amplifier noise. In addition, a general-purpose front end must have a differential input to work with booth differential and single-ended input signals [3], and nowadays a differential output is also desirable to provide a direct connection to high-resolution analog-to-digital converters (ADCs) with differential inputs. Then, a front end for a wide range of applications should be fully differential with very low voltage and current input noise levels. It is also desirable a decoupled feature, which is mandatory for dc signals, but also useful to optimize noise and dynamic range when amplifying very low-frequency voltages [4], [5]

There are commercially available integrated instrumentation amplifiers based on Bipolar Junction Transistors (BJT) as the INA849 and the INA851 of Texas Instruments with noise spectral densities $e_n$ as low as $1 \text{nV/}\sqrt{\text{Hz}}$, but present current noise spectral densities $i_n$ of around $1000 \text{fA/}\sqrt{\text{Hz}}$. In addition, there are fully-differential instrumentation amplifiers based on CMOS technologies as the LTC6373 of Analog Devices with $i_n=1 \text{fA/}\sqrt{\text{Hz}}$, but featuring $e_n=8 \text{nV/}\sqrt{\text{Hz}}$.

For now, the only way to achieve simultaneously low $e_n$ and $i_n$ values is by using an input stage composed by discrete JFETs. Designs based on this approach, that allows achieving voltage noise spectral densities $e_n$ below $1 \text{nV/}\sqrt{\text{Hz}}$ and current noise spectral densities $i_n$ of just a few tenths of $\text{fA/}\sqrt{\text{Hz}}$, have been proposed [6], [3]. They work on very low-frequency signals, but they cannot work on dc signals as some instrumentation applications require. The main characteristics of the mentioned alternatives are summarized in Table 1.

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An appropriate topology to implement low-noise fully-differential amplifiers, able to work from dc, is the current feedback scheme depicted in Fig.1. This beautiful topology is old but current and was introduced in the MODEL 601 Data Amplifier by Analog Devices in 1968 [7] and then implemented in several instrumentation amplifiers integrated circuits from the AD524 released in 1983 to the recent low-noise instrumentation amplifier AD849. It was also used in discrete implementations for microphone preamplifiers such as the Harrison PC1041 produced in 1978 [8] and the double-balanced version proposed in [9]. The circuit works in a closed-loop scheme for common-mode signals that set a collector bias current \( I_C \) and a collector voltage \( V_C \) independent of transistor parameters:

\[
I_C = \frac{(V_P - V_B)}{R_D}; \quad V_C = V_B
\]

and also for differential voltages, ensuring a well-defined gain \( G_a \) set by the fully-differential attenuator \( R_B, R_A, R_R \) and given by:

\[
G_a = 1 + \frac{2R_A}{R_B}
\]

In this circuit, power-supply voltages and the bias source \( V_B \) work as common mode generators and do not contribute to the overall noise. In addition, the input stage transistors operate at a constant collector voltage reducing the Miller effect.

Table 1. Comparison of the proposed circuit with other works.

<table>
<thead>
<tr>
<th></th>
<th>DC-Coupled F-D Fixed gain</th>
<th>TYPE</th>
<th>( e_n @1\text{kHz} ) [nV/\sqrt{Hz}]</th>
<th>( i_n @1\text{kHz} ) [fA/\sqrt{Hz}]</th>
<th>( C_{in} ) [pF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>YES</td>
<td>YES</td>
<td>YES JFET+OA</td>
<td>0.9</td>
<td>&lt;10</td>
</tr>
<tr>
<td>INA851</td>
<td>YES</td>
<td>YES</td>
<td>IC (BJT)</td>
<td>3.2</td>
<td>800</td>
</tr>
<tr>
<td>INA849</td>
<td>YES</td>
<td>NO</td>
<td>YES IC (BJT)</td>
<td>1.0</td>
<td>1100</td>
</tr>
<tr>
<td>LTC6373</td>
<td>YES</td>
<td>YES</td>
<td>IC (JFET)</td>
<td>8.0</td>
<td>1.0</td>
</tr>
<tr>
<td>[3]</td>
<td>NO</td>
<td>YES*</td>
<td>YES JFET+OA</td>
<td>1.0</td>
<td>50</td>
</tr>
<tr>
<td>[6]</td>
<td>NO</td>
<td>YES*</td>
<td>NO JFET+OA</td>
<td>0.8</td>
<td>&lt;10</td>
</tr>
</tbody>
</table>

*These circuits include a final stage to provide a single-ended output, but their front ends are fully differential (F-D).

All the implementations of the circuit in Fig.1, both with discrete components as by integrated circuits, have been made using a BJT input stage, leading to a somewhat high current noise spectral density. To remedy this, it is proposed to replace the BJT pair with JFET devices resulting in the circuit depicted in Fig.2. It presents some differences in the operating point behavior but inherits the excellent characteristics of the current feedback topology whereas featuring very-low bias and noise currents, thus extending its use to moderate or high impedance sensors. The proposal is simple but effective, its key is the availability of JFET devices with voltage noise spectral densities \( e_n \) similar to that of BJTs and current noise values \( i_n \) three orders of magnitude lower.

II. PROPOSED CIRCUIT

The proposed circuit, shown in Fig.2, can be seen as a JFET version of the circuit in Fig.1 or as a fully-differential obtained by mirroring the single-ended amplifier proposed in [4]. Being a fully differential circuit, inside it coexist common mode (CM) voltages that set the operating point and differential mode (DM) signals that are amplified. A proper circuit behavior must be ensured for both modes [10], [11].

A. Operation point analysis

The drain current \( I_D \) and the drain voltage \( V_D \) of the JFETs are imposed by the OA virtual ground and are given by:

Fig. 1. Fully-differential current feedback amplifier scheme. The common mode feedback ensures the transistors’ operating point regardless of their parameters, while the differential-mode feedback set a precise gain \( G_{in} = 1 + 2R_D/R_A \).

Fig. 2. Proposed fully-differential amplifier scheme. The common mode feedback ensures constant JFET bias current, while the differential-mode feedback set a gain \( G_{in} = 1 + 2R_D/R_A \) independent of the JFET parameters.
The relationship between \( I_D \) and the Gate-Source voltage \( V_{GS} \) can be approximated by a quadratic function given by:

\[
I_D = I_{DSS}(1 - V_{GS}/V_{GSC})^2.
\]

where \( I_{DSS} \) is the JFET saturation current, \( V_{GSC} \) is its cutoff voltage, and \( V_{GS} \) is the gate-source voltage. The OA output voltage \( V_O \) is given by:

\[
V_O = V_{IC} - I_D R_B - V_{GSC} \left(1 - \sqrt{I_D/IDSS}\right),
\]

where \( V_{IC} \) is the common mode input voltage. Typically, \( V_{GSC} \) is around -1 V and, to achieve low voltage noise spectral densities \( e_{FET} \), values of \( I_D \) close to \( I_{DSS} \) are used. Then, the last term in (5) can be neglected:

\[
V_O \approx V_{IC} - I_D R_B.
\]

This imposes the minimum \( V_{IC} \) admissible to avoid the OA output saturation at \( V_{OMIN} \):

\[
V_{IC} > V_{OMIN} + I_D R_B.
\]

The maximum \( V_{IC} \) that ensures a minimum drain-source voltage \( V_{DSNMIN} \) value and is given by:

\[
V_{IC} < V_{OMIN} - I_D R_B.
\]

Finally, the common mode input range can be expressed as:

\[
V_{OMIN} + I_D R_B < V_{IC} < V_{OMIN} - I_D R_B.
\]

This equation does not impose a hard restriction. For example, adopting typical parameters values as \( I_D=10 \) mA; \( R_B=500 \) Ω; \( V_{OMIN}=-10 \) V; \( V_{B}=6 \) V; \( V_{DSNMIN}=1 \) V, the amplifier will work properly with common mode input voltages \( V_{IC} \) between -5 V to +5 V.

B. Frequency response and stability issues

The topology is fully differential and its dynamic for CM and DM signals can be analyzed separately using the differential mode and the common mode equivalent half-circuits shown in Fig.3(a), and Fig.3(b), respectively [11]. Both half-circuits must be stable to ensure the stability of the overall circuit [10], [12].

C. Common mode stability and frequency response

Disregarding the capacitor \( C_F \) and solving the circuit of Fig.3.b, the common mode closed-loop gain \( G_{CC}(s) = V_{oc}(s)/V_{ic}(s) \) results:

\[
G_{CC}(s)|_{CF=0} = \frac{g_m R_B}{1 + g_m R_B A(s)},
\]

where the open loop gain is given by:

\[
G(s) = \frac{g_m R_D}{1 + g_m R_B A(s)}.
\]

The worst case corresponds to the lower value of \( R_B \) and is \( G(s) = g_m R_D A(s) \): the OA open loop gain is increased by a factor \( g_m R_D \) and the circuit becomes unstable. This shows the necessity of including the capacitor \( C_F \). By so doing, the OA works as an integrator for the drain’s current, the open loop gain is \( G_{OL}(s) = g_m/sC_F g_n \), and (11) becomes:

\[
G_{CC}(s) = \frac{1}{1 + sC_F (g_m^{-1} + R_B)}.
\]

The circuit presents a first-order transfer function. It is stable, with a unity gain for low frequencies and a cutoff frequency \( f_c \) given by:

\[
f_c = \frac{1}{2\pi C_F (g_m^{-1} + R_B)}.
\]

D. Differential mode stability and frequency response

For differential mode voltages, the circuit works like its single-ended version analyzed in [4], which exactly matches the DM circuit in Fig.3(a). It does not present stability problems, even without \( C_F \), when a closed-loop gain \( G_n \) greater than \( g_m R_B \) is set, but this capacitor must be included to ensure common mode stability and the differential closed-loop gain \( G_{DD}(s) = V_{oc}(s)/V_{id}(s) \) results in [4]:

\[
G_{DD}(s) = \frac{G_n}{1 + sC_F G_n / g_m},
\]

thus, verifying a first-order response with a low-frequency gain \( G_n \) and a -3 dB cutoff frequency \( f_c \) given by:

\[
f_c = \frac{g_m}{2\pi C_F G_n}.
\]

E. Amplifier noise Analysis

The differential mode noise of the proposed circuit can be analyzed from its differential mode half-circuit [13] depicted in Fig.4. Note that this circuit is similar to that of the single-ended amplifier in [4], with the advantage that noise sources such as the power supply and the bias voltage \( V_B \) act as common-mode sources and do not contribute significantly to the overall amplifier noise. The capacitors \( C_F \) were omitted because they do not affect the amplifier noise gain within its bandwidth.
The term \(a\) few expresses the noise spectral density with just a change of units
transfer functions within the bandwidth of interest and (18) also
in the same way [13] and finally, the input referred overall
statistically independent, the mean square value
by
respectively. The OA voltage and current noises are modeled
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\(e_{RA}\) and \(e_{NA}\) sources. Solving the circuit in Fig.4 to obtain
the output noise \(e_{o}\) and then referring it to the input, the input
referred noise \(e_{IH}\) of the half circuit is given by:

\[
e_{IH} = e_{FET} + e_{RA/2} + \frac{e_{RB}}{G_n} + \frac{i_{NA}}{g_m} + \frac{e_{RD} + e_{NA}}{g_m R_D}. \tag{16}
\]

The above equation is valid for instantaneous values of
deterministic signals, but stochastic signals as noise are
described by statistical features such as standard deviation in
Volts RMS or spectral densities expressed in \(V^2/Hz\) or
\(V/\sqrt{Hz}\). Assuming that the different noise sources in (16) are
statistically independent, the mean square value \(e_{IH}^2\) is given by:

\[
e_{IH}^2 \approx e_{FET}^2 + e_{RA/2}^2 + \left(\frac{e_{RB}}{G_n}\right)^2 + \left(\frac{i_{NA}}{g_m}\right)^2 + \frac{e_{RD}^2 + e_{NA}^2}{(g_m R_D)^2}. \tag{17}
\]

This result represents the contributions of the components
of one half of the circuit. The other half of the circuit contributes
in the same way [13] and finally, the input referred overall
differential mode noise \(e_I^2\) is given by:

\[
e_I^2 \approx 2e_{FET}^2 + e_{RA}^2 + 2\left(\frac{e_{RB}}{G_n}\right)^2 + 2\left(\frac{i_{NA}}{g_m}\right)^2 + \left(\frac{e_{RD}^2 + e_{NA}^2}{(g_m R_D)^2}\right). \tag{18}
\]

Being dc-coupled, the proposed circuit presents constant
transfer functions within the bandwidth of interest and (18) also
expresses the noise spectral density with just a change of units
from \([V^2]\) to \([V^2/Hz]\).

Considering that, even for bipolar OA devices, \(i_{NA}\) is of just
a few pA/\(\sqrt{Hz}\) and \(g_m\) values of tens of mS, the term \(i_{NA}/g_m\) results
of the order of tenths of nV/\(\sqrt{Hz}\) can be neglected.
The term \(e_{RB}/G_n\) can also neglected against \(e_{RA}\) because
\(e_{RB}/G_n << e_{RA}\) and \(e_{I}^2\) can be approximated by:

\[
e_{I}^2 \approx 2e_{FET}^2 + e_{RA}^2 + \frac{e_{RD}^2 + e_{NA}^2}{(g_m R_D)^2}. \tag{19}
\]

The gain \(g_m R_D\) provided by the JFET stage is around 20-30
times and as can be seen from (19), it relaxes the noise
constraints for \(e_{RD}\) and \(e_{NA}\) and the input-referred noise can be approximated by:

\[
e_I^2 \approx 2e_{FET}^2 + e_{RA}^2. \tag{20}
\]

The noise of \(R_A\) appears directly at the input, but the proposed
topology allows using very low \(R_A\) values of just a few ohms.
In this case, its effects can be neglected, and the overall
amplifier noise is dominated by the JFET voltage noise leading to:

\[
e_i = \frac{\sqrt{2} e_{FET}}{\sqrt{N}}. \tag{21}
\]

Then, the amplifier noise is almost exclusively due to the
voltage noise of the JFET. This is an important feature: the
amplifier noise can be reduced by reducing the JFET noise. This
can be made by selecting low-noise devices or by using several
JFETs in parallel. It seems obvious, but in the case of single-ended
circuits it is not enough to connect JFETs in parallel but
rather complete amplifiers, because otherwise the noise
contributions of \(V_b\) and \(V_p\) become significant [4]. For this
differential topology, when connecting \(N\) JFETs in parallel the
input-referred amplifier voltage noise \(e_i\) reduces \(\sqrt{N}\) times
while the current noise \(i_i\) increases in the same factor [14]:

\[
e_i = \frac{\sqrt{2} e_{FET}}{\sqrt{N}}; \quad i_i = \frac{\sqrt{2} i_{FET}}{\sqrt{N}}. \tag{22}
\]

There are JFETs as the IF3602 of InterfetTM that feature
very low \(e_{FET}\) values, but present huge input capacitances, of
several hundreds of pF, thus limiting the amplifier bandwidth
in front of moderate or high source impedances; and huge input
offset voltages, up to 100 mV, that force to ac-coupling input
stages [2], [3] to set a significant gain at the front end.
Additionally, these devices are very expensive. Then, the use of
several JFETs in parallel is a good choice and provides an
additional design variable: the number \(N\) of JFETs in parallel to
solve the tradeoff between voltage noise, current noise, input
capacitance, and power consumption.

III. DESIGN EXAMPLE

As an example, a fully differential instrumentation amplifier
to act as a front end for measuring instruments is depicted.
The main features are a nominal gain \(G_n=60\) dB, a signal bandwidth
BW from dc to 100 kHz, a voltage noise \(e_i<1\) nV/\(\sqrt{Hz}\)
@1 kHz and a current noise \(i_i<10\) fA/\(\sqrt{Hz}\) @1 kHz.

To achieve \(e_i<1\) nV/\(\sqrt{Hz}\) at 1 kHz the JF2140 of Texas
Instruments was selected, which presents \(e_{FET}=0.9\) nV/\(\sqrt{Hz}\)
@1 kHz for \(I_D=7\) mA [4]. Larger \(I_D\) currents result in slightly
lower \(e_{FET}\) values but demand significant output currents on the
OAs. With just a JFET pair \((N=1)\) the input-referred noise
predicted by (21) is \(e_i \approx \sqrt{2} e_{FET} = 1.2\) nV/\(\sqrt{Hz}\) @1 kHz. To
reduce \(e_i\) bellow \(1\) nV/\(\sqrt{Hz}\) @1 kHz two JFETs per side \((N=2)\)
were connected in parallel, and the expected input noise reduces to
\(e_i \approx \sqrt{2} e_{FET} = 0.9\) nV/\(\sqrt{Hz}\) @1 kHz. The current
input noise of the JFE2140 is of 1.6 fA/√Hz@1 kHz and results in an estimated amplifier current noise $i_i \approx 2.3$ fA/√Hz@1 kHz, lower than 10 fA/√Hz@1 kHz. A resistor $R_A=1 \Omega$ was used to neglect its contribution to the amplifier noise and $R_B=500 \Omega$ to ensure a gain of 1001 times (≈60 dB). To achieve a signal bandwidth of almost 100 kHz, according to (15) and considering $g_m=30$ mS, the capacitor $C_F$ must be lower than 32 pF, thus $C_F = 20$ pF was adopted. In order to avoid the noise contribution of the resistor $R_D$ and the OA voltage noise $e_{nA}$ according to (19), $R_B=500 \Omega$ ($e_{nD}=2.8$ nV/√Hz) and the OPA211 was selected ($e_{nA}=1.1$ nV/√Hz@1 kHz). The circuit was powered at ±12 V and a drain bias voltage $V_B=5$ V was used to set a drain current $I_D=7$ mA on each JFET.

IV. EXPERIMENTAL RESULTS

Figure 5 shows the circuit diagram of the implemented amplifier. As predicted by (6), its output exhibits a CM bias voltage of around –7 V, and a CM restoration circuit was introduced to remove this potential, thus relaxing the acquisition of the amplifier output. This circuit ensures a zero CM output voltage and corresponds to an inverter version of the scheme published in [15]. For this purpose, a fully differential commercial OA such as the THS4130 can also be used.

A. DC parameters

Imposing a short circuit at the amplifier input, it outputs a differential voltage $v_{ad}=-1.35$ V. Then a resistor of $R=1$ MΩ was connected at one input resulting in $v_{ad}=-1.13$ V, that increases to $v_{ad}=-1.32$ V for $R=10$ MΩ. These measurements suggest an input voltage offset $v_{OFFSET}=-1.35$ mV and an input bias current $I_{BIAS}=2.7$ pA. These values agree with that expected from the JFE2140 datasheet [16].

B. Amplifier noise

The experimental setup for the measuring of the amplifier spectral density noise is shown in Fig.6. For a nominal gain $G_n=100$, a differential ac-coupling network [17] and an instrumentation amplifier were added to increase the amplifier output before its connection to the spectrum analyzer (Agilent 35670A). For this test, the amplifier was powered by batteries and enclosed in a shield box.

The amplifier input-referred spectral noise density $e_i$ with one JFET pair and two JFET pairs are shown in Fig.7. Note that in the first case $e_i@1$ kHz is greater than 1 nV/√Hz, but by connecting two JFET in parallel reduces to 0.9 nV/√Hz as (22) predicts. In both tests, each transistor was biased at $I_D=7$ mA by changing $R_D$ from 1 kΩ to 500 Ω.
A second test was performed varying the nominal gain $G_n$ from 60 dB ($R_u=1 \Omega$) to 40 dB ($R_u=10 \Omega$) and the corresponding spectral densities are shown in Fig. 8. It can be observed that for $G_n=40$ dB the noise increases but remains below 1 nV/√Hz@1 kHz. This behavior is compatible with the 0.4 nV/√Hz noise contribution of $R_u=10 \Omega$: $\sqrt{0.4^2+0.9^2} \approx 0.98$ nV/√Hz@1 kHz.

Finally, to evaluate the amplifier current noise $i_i$ and its input capacitance $C_{in}$, a resistor $R$ was connected to one input keeping a short circuit in the other one. Figure 9 shows the noise spectral densities for $R=1$ MΩ and $R=10$ MΩ. For low frequencies, the voltage noise densities agree with the theoretical thermal resistor noise $e^2_{R}=4kTR$ and then decay because the low pass filter $R$ composes with $C_{in}$. In dashed line is indicated the expected spectral density for $C_{in}=23$ pF, whose good agreement with the experimental data can be taken as an estimation of the $C_{in}$ value. The spectrum estimation resolution for $R=10$ MΩ is around 10 nV/√Hz, and no significative difference between the thermal noise of the resistor (41 μV/√Hz) and the experimental data is observed. This indicates that the input current noise $i_i$ is below 10 fA/√Hz, which is in accordance to the reported JFE2140 parameter $i_{FET}=1.6$ fA/√Hz, that considering $N=2$ (two JFET in parallel) results in $i_i=\sqrt{2}1.6$ fA/√Hz = 2.25 fA/√Hz.

C. Frequency response

The amplifier frequency responses for $G_n=60$ dB and $G_n=40$ dB are shown in Fig. 10. The experimental measurements, indicated in circles, were performed by an Agilent DSO-X 2024A digital oscilloscope with its embedded function generator. The frequency response given by (15) and that obtained by simulation with TINA software of Texas Instruments are also indicated. All the curves show a very good match between them considering a JFET transconductance $g_m=28$ mS.
V. CONCLUSIONS

Hybrid amplifiers composed by a JFET input stage and OA allows achieving fully differential amplifiers with voltage noise spectral densities below 1 nV/√Hz and current noise densities below 10 fA/√Hz by using low-cost general-purpose devices. These simultaneously low voltage and current noise levels cannot be achieved with current integrated circuits. Single-ended topologies lead to lower noise levels, but power supply and bias voltage must be decoupled with very large capacitors because they contribute to the overall amplifier noise. When a fully differential topology is used, these sources produce common mode signals and do not contribute to the amplifier noise. In the first case, to reduce noise effectively, several amplifiers must be connected in parallel, whereas in the second one by just connecting N JFETs in parallel the overall voltage noise is reduced by a √N factor.

A hybrid JFET fully differential amplifier based on the current feedback scheme is proposed. It provides closed-loop control of common-mode (CM) and differential mode voltages (DM). The first ensures a fixed drain current independent of the transistor parameters and a fixed drain voltage, thus reducing the Miller effect. The DM loop sets a precise differential gain as instrumentation applications demand. Because amplifier biasing and amplifier signal processing correspond to different and independent modes, large capacitances are not needed to decouple AC signals, allowing the implementation of DC-coupled amplifiers.

A complete stability analysis of the proposed circuit and its design equations are presented. As an example, a fully-differential amplifier with $G_m = 60$ dB, $g_{m} = 0.9$ nV/√Hz at 1 kHz, $I_C < 10$ fA/√Hz at 1 kHz and a bandwidth of 100 kHz was designed, built and tested. The experimental data shows a very good agreement against simulation and the analytic design equations, thus validating them and allowing the amplifier design to be adapted to different needs.

VI. REFERENCES