Low Power and High-Speed Multi-Threshold CMOS-Data Flip-Flop Design Validation on 90nm Technology Node Using EDA Tools

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Abstract

The primary focus of Research VLSI Technology is to optimize power and Delay, so that a low power and High Speed Designs are obtained. The MTCMOS is one of the Such Promising CMOS Chip technology that uses transistors with multiple threshold voltages to optimize power and Delay. Subthreshold Leakage has brought down and achieved power optimization. In this article Multi threshold CMOS based Data Flip-Flop is Designed, analyzed and Validated on 90 nm Technology Node Using EDA Tools.
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Abstract—The primary focus of Research VLSI Technology is to optimize power and Delay, so that a low power and High Speed Designs are obtained. The MTCMOS is one of the Such Promising CMOS Chip technology that uses transistors with multiple threshold voltages to optimize power and Delay. Subthreshold Leakage has brought down and achieved power optimization. In this article Multi threshold CMOS based Data Flip-Flop is Designed, analyzed and Validated on 90 nm Technology Node Using EDA Tools.

Index Terms—VLSI-Very Large scale of Integration, MTCMOS-Multi threshold Complementary metal oxide semiconductor, EDA-Electronic design Automation.

I. INTRODUCTION

Low power and high speed devices are in more demand now a days, in this work we have the designed would D-flipflop Using the MTCMOS technique, which will Avoid the sub threshold Leakage[1] current in the MOS transistor while standby mode, this concept is also called as the POWER GATING, This work has been done in the cadence Virtuoso.

II. MTCMOS TECHNIQUE

MTCMOS is technique in which the threshold voltages of the both NMOS and PMOS transistors are different, this technique is mainly is used to reduce the subthreshold leakage of MOS transistor[2][3] in standby mode (sleep mode). The MTCMOS technique can be operated in two modes High Threshold mode and Low threshold mode, in high Threshold mode it can be minimize the subthreshold[5] leakage and Low threshold mode can optimize the speed of the circuit.

III. DESIGN VALIDATION USING EDA

The data Flip-Flop is also called as the Delay flipflop, it is used in the communication circuits where the delay requires to synchronize the signals with another signal, in this work we[4][5] designed the data flipflop with the MTCMOS technique using the gpdk 90 nm Technology to reduce the subthreshold leakage of the circuit while in standby mode and to increase the speed of the circuit.
Fig-2 MTCMOS Based Data Flip-Flop

The above circuit shows the Data flip-flop using MTCMOS Technique designed on 90nm technology node, the above MOS are operated upto 1.2v to 1.8v of supply voltage.

The Following table shows the switching action of the MOS transistors. And the output of the data flip-flop according to the given input.

<table>
<thead>
<tr>
<th>CLK</th>
<th>Input</th>
<th>Stand</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>M7</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
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<td>OFF</td>
<td>ON</td>
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<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>1</td>
</tr>
</tbody>
</table>

Table-1 Switching action of MOS Transistors

III.1 MOS TRANSISTOR CHARACTERISTICS:

The below fig shows the MTCMOS Based Data flip-flop layout with 90nm technology Node.
The following fig shows the Ids vs. Vds relation of PMOS-BSIM in MTCMOS configuration.

Fig-7 PMOS Ids vs Vds relationship in MTCMOS

The following fig shows the Ids vs. Vg relation of PMOS-BSIM in MTCMOS configuration.

Fig-8 PMOS Ids vs Vg relationship in MTCMOS

The following figure shows the threshold voltage of NMOS-BSIM in the MTCMOS configuration.

Fig-9 Threshold Voltage of NMOS

Based on the above characteristics, it is observed that the multi-threshold voltage for NMOS and PMOS was effectively adopted in this work.

V. RESULTS

The following figure shows the schematic of a MTCMOS-based data flip-flop.

Fig-10 Schematic of MTCMOS Data Flip-Flop with 90nm Tech node

The following Fig. shows the transient analysis of the MTCMOS-based data flip-flop.

Fig-11 Transient response of the MTCMOS Based Data Flip-Flop

The following Fig. shows the layout of a MTCMOS-based data flip-flop on a 90-nm design role in the Microwind Tool.

The following Fig. shows the layout of a MTCMOS-based data flip-flop on a 90-nm design role in the Microwind Tool.

Fig-12 Overall Power Consumed by MTCMOS Based Data Flip-Flop
The above figure shows the overall power consumption of the MTCMOS-based data flip-flop, which is 46.754 uWatts.

The following figure shows the rise time and fall time delays in the MTCMOS-based data flip-flop.

Fig-13 Propagation Delay at Rising Edge of MTCMOS Based Data FlipFlop

The above figure shows the propagation delay at the rising edge, which is 501.3348 fs.

Fig-14 Propagation Delay at Rising Edge of MTCMOS Based Data Flip-Flop

The above figure shows the propagation delay at the rising edge, which is 138.71 fs.

VI. CONCLUSION

In this work, a low-power multi-threshold CMOS D flip-flop design is validated with the following:

- **Effective Multi-Thresholding:** It is clearly observed that for NMOS Threshold Voltage is in the range of -0.60 volts, for PMOS Threshold Voltage is in the range of 0.60 - 3.10 volts, and the same has been observed in their characteristics.
- **In the MTCMOS Design D Flip-Flop:** sub-threshold leakage is considerably minimized, and overall power is optimized to 46.754 uWatts.
- **Rise time, fall time delay** Analyzed and Obtained as Rise Time in Order 501.3348fs, Fall Time in Order 138.71fs

Therefore, the proposed method is a low-power, high-speed MTCMOS data flip-flop based on all the analysis done in the EDA tools.

VII. REFERENCES

[5] M. W. Rahman Khan and M. Mohiuddin Uzzal, "Multi-Threshold CMOS Devices: A Comparative Analysis of Leakage Power and Delay in Digital Circuits for Nano-Scale Technology." 2019 2nd International Conference on Innovation in Engineering and Technology (ICIET), Dhaka, Bangladesh, 2019, pp. 1-6, doi: 10.1109/ICIET48527.2019.9290556. keywords: {Threshold voltage;Leakage currents;Logic gates;Delays;Clocks;CMOS technology;Inverters;MTCMOS;VLSI;threshold voltage;nanotechnology;leakage power;delay;power delay product;D flip flop},