A 3D Photon-to-Digital Converter Readout for Low-Power and Large-Area Applications

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Abstract: The new trend in large area noble liquid experiments is to measure the scintillation light with photodetectors and their electronics inside the active volume. Compared to the typical approach of using silicon photomultipliers (SiPM) with the analog readout chain to an analog-to-digital converter, this paper presents a new 3D photon-to-digital converter (PDC) readout that takes advantage of the binary nature of the single-photon avalanche diode. The readout contains 4096 pixels over 25 mm$^2$, each including a 3D bonding pad and a quenching circuit. The readout features three different outputs: a fast flag to get the timestamp of each event from an external time-to-digital converter, a digital sum to retrieve the number of pixels triggered during an event and an analog monitor to generate an analog SiPM-like output. The analog monitor is also used to validate the two former digital outputs. The readout also includes 61 2D CMOS SPADs for validation purpose prior to the final 3D integration with a Teledyne DALSA custom SPAD array. As a first system integration toward large-area detector applications, a mini-tile of $2 \times 2$ readouts has been developed to test all the functionalities. The measured single-photon timing resolution ranges from 72 to 93 ps FWHM across the mini-tile SPAD channels population (i.e. $4 \times 61$ channels). The flag timing resolution is below 95 ps RMS, which includes the contribution of the optimized flag H-tree with an additional trigger tree to replace the 3D SPAD array for 2D testing. Once bonded with the 3D SPADs, the trigger tree won’t be required to measure the flag timing resolution. With the removed contribution of the trigger tree, the estimated flag timing resolution should be below 45 ps RMS. The benefits of the digital sum output depend on the application, and this paper focuses on two cases. First, a low-power coincidence scheme for the nEXO liquid xenon experiment, leading to a power consumption as low as 140 µW per PDC. On the other hand, with a finer sampling mode of the scintillation light for pulse shape discrimination in liquid argon, the power consumption remains below 100 µW per PDC. Overall, this readout is designed as a replacement for a typical analog SiPM chain, without any compromise on the performances.

Keywords: Single-Photon Avalanche Diode; SPAD Array; SiPM; Silicon Photomultiplier; Digital SiPM; 3D Photon-to-Digital Converter; Liquid Argon Detector; Liquid Xenon Detector

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1 Introduction

In particle physics, the mass of the neutrino and the origin of dark matter are trending subjects. Collaborations around the globe are working with large scale noble liquid detectors to answer those questions [1–5]. The recent developments in silicon photomultipliers (SiPM), including better photodetection efficiency with improvement targeted at the VUV spectrum and lower dark noise [6–9], bring new opportunities to replace photomultiplier tubes (PMT) which are still used by some experiments [10, 11]. However, collecting rare photons over multiple square meters at cryogenic temperature is not trivial. Since the photosensors and the readout electronics are soaked in noble liquid, the power consumption must be kept very low to prevent boiling or convection. Special care must be taken in the selection of the components to reduce background signals or noise sources, which affect the experiments’s light yield, signal-to-noise ratio and energy resolution. The typical approach is to use silicon photomultipliers read out by a pre-amplifier, a shaping amplifier and then an analog-to-digital converter (ADC) to digitize the output [12]. This type of solution has shown a timing resolution better than 10 ns [13] for background discrimination in liquid argon.

In this paper, we present a new digital readout for a 3D photon-to-digital converter (PDC), designed to work in low-power and large-area systems such as particle physic experiments. The 3D PDC consists of a single-photon avalanche diode (SPAD) array vertically integrated with a CMOS readout layer where each SPAD is connected individually to its quenching circuit. The 3D integration process of the PDC is done at wafer-level to allow large-scale manufacturing [14, 15]. For large-scale experiments, PDCs will be assembled in tiles to increase the photosensitive area and to facilitate system integration into photodetection modules (PDM). Each tile will contain another CMOS circuit called the tile controller, to manage communication between the PDCs and the external acquisition system (DAQ).

The 3D PDC CMOS readout ASIC takes advantage of the digital nature of the SPAD. It contains embedded digital logic to process its 4096 pixels. Section 2 presents the readout ASIC architecture including the pixel-level electronics and the outputs aimed at different applications. Section 3 gives a description of the test setup and how the measurements are obtained. Section 4 focuses on the achievable timing jitter, the output capabilities and the power consumption of the PDC readout ASIC. This leads to a discussion in section 5 on the power consumption for different application cases as well as system-level integration consideration for large-area detectors based on the 2 × 2 PDC array presented in this paper.

2 Architecture

2.1 Overview

This 3D PDC readout ASIC is designed in the TSMC 180 nm BCD process. The total die size is 5.3 × 5.85 mm² and the area to receive 3D integrated SPADs is 5 × 5 mm² (Figure 1). The pitch in the array is 78 µm, resulting in a 64 × 64 pixels design. Each pixel contains a 3D bonding pad and a quenching circuit (QC). To test the readout without the final 3D assembly to the custom SPADs tier, a row of 61 2D integrated CMOS SPADs is included for validation purpose. This readout provides three complementary outputs that give information on the number of triggered pixels, that are a flag output, a digital sum and an analog current sum (Figure 2).
Figure 1: Top view of the PDC readout with the 61 internal SPADs shown at the top section, the 4096 pixels with their bonding pad in the middle section and the 32 wire bonding pads at the bottom section. The die size is $5.3 \times 5.85 \text{ mm}^2$.

Figure 2: Block diagram of the PDC CMOS readout (yellow) including the 3D SPAD array on the left (blue) and the PDM tile controller on the right (green). The CMOS readout contains 3D bonding pads, 61 integrated 2D CMOS SPADs and 4096 passive QCs. The outputs of each QC are combined together to form the three PDC’s outputs: a digital sum, a flag and an analog monitor.

2.2 Integrated 2D CMOS SPADs for Validation Purposes

The integrated 2D SPADs are used for functional testing and are not the one to be used in the final 3D stack. All the tests involving SPADs in the present work were done with the 2D internal CMOS SPADs. Their active area diameter is $34 \mu\text{m}$, resulting in a fill factor per SPAD of 17%. All of these 61 SPADs are connected to a passive quenching circuit.
2.3 Quenching Circuit

Since the primary objective is to bond the readout to a tier of SPADs in 3D, each quenching circuit contains an interconnection pad on the top metal layer. The QC architecture is designed for SPAD cathode reading (Figure 3). To improve the dynamic range of the SPADs by extending the excess voltage up to 10 V while using only 5 V transistors, a cascode transistor (M3) is placed between the input pad and the discriminator (U1)[16, 17]. To reduce static power consumption, this design uses an inverter over a comparator for the leading edge detection. It also features a pixel enable/disable circuit (M4 and U2) to turn off noisy or damaged pixels. A trigger tree allows the characterization of each individual pixel through the transistor M5 that emulates a SPAD event. Transistor M6 disables the trigger during the recharge to prevent short circuits in the front-end. The hold-off delay can be adjusted in duration to reduce the afterpulsing at the expense of a loss in photosensitive time [1, 18, 19]. To accommodate different SPAD parasitic capacitance, a second monostable can set the recharge time between 2 ns and 60 ns. Each quenching circuit generates three signals that are combined to produce the three different outputs of the PDC: a flag signal for precise timing measurements or coincidences (section 2.4), a digital sum (section 2.5) and an analog current source for the analog monitor (section 2.6).

Figure 3: Illustration of a single pixel of the array with a cathode reading QC and an inverter-based discriminator. The QC feeds the three different outputs of the PDC: a flag with an adjustable pulse width for timing measurements, a signal activated for the duration of the hold-off to be used for the digital sum and an adjustable current source for an analog sum.

2.4 Flag

The 4096 pixels are combined for the flag signal using an OR gate tree (Figure 4). This output does not require any clock signal to work and propagates as soon as a pixel triggers, hence is purely asynchronous and low-power. A monostable (Figure 3) generates a pulse width adjustable between 2 ns and 60 ns. To reduce the flag jitter when using an external time-to-digital converter (TDC), the path and delay for each pixels to the flag output must be accurately matched. The flag pulse therefore propagates through an H-tree optimized with a custom script with a precisely placed OR.
gate in each junction [20]. This optimization has been made to reduce the flag time propagation variation as a function of position that would translate into a system jitter. Another purpose of the flag is to implement a dark count filter when using multiple PDCs on a tile in a large experiment. In this case, the digital sum is sent out only when multiple PDCs trigger inside a coincidence window, hence ignoring local asynchronous dark count from any PDC.

![Diagram of OR gate cells](image)

**Figure 4**: Position of each OR gate cell to generate the H-Tree with matched propagation delay for each pixel to the flag output.

### 2.5 Digital Sum

A digital sum provides the number of detected photons and can be read on request by the tile controller. When the acquisition signal is sent, it freezes the status of each pixel to digitally sum how many pixels have triggered. Instead of counting the number of flags, this approach allows for multiple pixels to trigger at the same time without saturating. This results in a full dynamic range from 0 to 4096 pixels. An external signal controls the sum so it can be sampled once or with a continuous sampling rate with a minimum bin size of 10 ns. The sampling rate is dynamically tunable by the acquisition signal from the controller (e.g. 10 fast samples at 10 ns then 20 slow samples at 100 ns sampling rate). An internal FIFO with a depth of 128 bins stores the results and then transmit them to the tile controller. The operation of the sum requires a clock to process the result which increases the power consumption. Section 3.4 presents a coincidence window acquisition scheme to only read the digital sum when required.

### 2.6 Analog Monitor

The readout includes an analog output [21]. It is comparable to the output of an analog SiPM and is used to validate the result of the flag and the digital sum. It could also be used in some applications. Based on the approach proposed by Nolet [22], an adjustable current source from 0 to 30 µA in each pixel is enabled when the corresponding pixel triggers for the duration of the
hold-off delay. The total output current of the PDC is then proportional to the number of triggered pixels. The current sources are implemented with matched transistors from one pixel to another, enabling precise current and duration sent at the output. This way, the single-photon spectrum has high peak-to-valley ratio for the entire dynamic range. In comparison with an analog SiPM, the junction capacitance and the breakdown voltage variations blur the single-photon spectrum at higher count rates due to SPAD-to-SPAD gain variation. Here, the QC acts like a classic leading edge discriminator where the SPADs have a gain in the order of $10^3$ to $10^6$ [23]. The QC hence generates a swift signal with very fast rise time. The digital approach hereby presented takes advantage of the one-to-one readout for immunity with respect to SPAD characteristic variation [24]. Another benefit of the analog monitor is its direct compatibility with analog SiPM readouts. By using a transimpedance amplifier and an oscilloscope or an ADC, this signal can be compared to the result of the digital sum directly output by the PDC.

2.7 System Integration

The PDCs’ main purpose is to be integrated in an array to obtain large light detection tiles. The tile provides a mechanical support as well as an interface to interconnect PDCs to a dedicated tile controller. The latter sends configurations to the PDCs, manage the acquisitions, collects the number of photons and adds a timestamp to them. Different architectures can be used for the TDC to be implemented in the tile controller and good timing can be achieved with low power consumption [25]. This tile controller will improve the integration of the PDM by avoiding the connection of each individual PDC to an external acquisition system. The tile controller for the $2 \times 2$ PDCs prototype presented in this paper is implemented within an FPGA to provide an early proof-of-concept. A custom integrated circuit will be used in the final design.

3 Materials and Methods

The test platform (Figure 5) implements a $2 \times 2$ array of PDCs called the PDC head PCB. A Zynq UltraScale+ System-on-Chip (SoC) from Xilinx [26] acts as the tile controller. This SoC includes an FPGA for the interface to the PDCs and an ARM processor for the user interface and data management. The Zynq is on a separate custom development board connected through a flat cable to reduce the size of the tile. This approach facilitates the use of the head PCB into optical and cryogenic setups for characterization.

The head includes the readout for the analog monitor current output of $30 \, \mu A$ per pixel to convert and amplify it. A 13 GHz and 40 GSa/s scope (Agilent MSO-X91304A) acquires this signal and the flag for comparison with the digital sum of the PDCs.

3.1 SPAD Characteristics

The SPAD dark count rate (DCR), afterpulsing (AP) and photodetection efficiency (PDE) are measured using the zero photon probability (ZPP) [27] adapted to digital SiPM as described in [19]. The DCR and PDE are measured for each SPAD individually, thus disabling the other SPADs, removing the crosstalk contribution in the characterization. This method leaves the AP as the sole contributor to the correlated noise, facilitating its identification. A large-band halogen lamp coupled to a Horiba iHR320 is used as a source for the PDE measurement. The PDE is measured at a
SPAD excess voltage of 8 V and wavelength from 400 nm to 1000 nm and is compared to a PDM from Micro Photon Devices [28]. The SPAD single-photon timing resolution (SPTR) is measured with a Spectra Physics Mai Tai 80 MHz Ti:Sapphire pulsed laser. The timing jitter histograms are acquired with a Teledyne Lecroy SDA 6000A oscilloscope, and a Becker & Hickl PHD-400 fast diode as the reference timing detector. The test setup contribution is measured at 3 ps FWHM [16].

3.2 Flag Timing Resolution

The timing resolution of the flag output signal is measured using the PCB test setup described in Figure 5 and a Swabian Instruments Time Tagger Ultra [29]. The trigger signal is sent from the FPGA to the M5 transistor of the QC (Figure 3) through a trigger tree in the ASIC. A script implemented in the FPGA allows for the consecutive enabling of each of the 4096 pixels to characterize their individual contribution to the global timing resolution. The FPGA sends the trigger signal to both the ASIC and the Time Tagger Ultra to produce a histogram of the time delay for each pixel, from which the timing jitter and timing delay is extracted. The flag timing resolution is the combination of all these histograms, including the jitter and time delay.

3.3 Comparison of the Outputs

To use the PDC as a system and take full advantage of the three complementary outputs, they are first compared to better understand how they work. The block diagram in Figure 6 presents the connections between the test setup and the other required equipment. The light source is a green LED (SML-LX15GC-RP-TR) connected to a pulse generator (Berkeley Nucleonics 745) to drive a very low current through the LED with an adjustable pulse width. This light source is facing the 4 PDCs of the head PCB. A dark count filter algorithm is implemented inside the FPGA to trigger a PDC acquisition only on light pulses. This algorithm consists in detecting a programmed number
of events through the flag signal inside a given coincidence window. The oscilloscope digitizes the LED enabling signal, the analog monitor readout output, the flag and the acquisition signal. The digital sum of the PDC is synchronized and validated with the waveforms of the oscilloscope using post-processing.

**Figure 6**: Block diagram of the test setup used for the comparison of the three outputs, the coincidence window acquisition scheme and the continuous sampling capabilities. A pulse generator activates the LED to generate photons. The LED signal, the analog monitor (AM) and the flag outputs are directly connected to the oscilloscope. The acquisition signal from the controller is sent to both the PDCs and the oscilloscope to get a reference point to align the oscilloscope signals with the digital sum from the PDC in post-processing.

### 3.4 Coincidence Window Acquisition Scheme

To mitigate the dark count rate of the SPADs that would trigger undesired acquisitions, a dark count filter is implemented based on a coincidence scheme. Configurable inside the tile controller, a number of photons must be detected under a given period of time to trigger an acquisition, or the triggered pixels are ignored. For this acquisition scheme, the setup in Figure 5 is used. To produce only a few photons, the LED is turned on for 100 ns. The coincidence window and PDC hold-off time are both set to 500 ns. A flag detection threshold of three is programmed into the FPGA. The acquisition gets a single sample of the digital sum at the end of the coincidence window if the threshold is exceeded.

### 3.5 Continuous Sampling Capabilities

In liquid argon, the different time constants between the singlets (6 ns) and the triplets (approximately 1300 ns to 1600 ns) help to discriminate events with the same level of energy but with a different waveform in time [30]. Hence, the PDC can be sampled continuously. These samples, from a single PDC or summed over a larger area of PDCs by the tile controller, can then be used for pulse shape discrimination. Since the maximum sampling frequency of the PDC is larger than its maximum data transmission rate, each PDC saves the counts to its internal 128 bin FIFO.
To store events with duration longer than 10 µs while keeping a 10 ns sampling for the prompt photons, a dual sampling mode is required in the PDC. Samples are first saved in the PDC’s internal FIFO on each 10 ns clock cycle for a programmed number of bins. Then, the remaining of the sampling is done every $N$ clock cycle. The number of fast samples at each clock cycle, the number of slow samples and the spacing between each sample is programmed into the tile controller for more flexibility. With the configuration of the test setup described in Figure 5, the LED is turned on for 200 ns. The coincidence window is set to 50 ns and the detection threshold is 2. Here, considering the light signature of the LED over 2.5 µs, the acquisition is composed of 50 fast samples and 50 slow samples with a respective sampling period of 10 ns and 50 ns.

3.6 Power Consumption

The power consumption of the PDC in operation is measured through current sense resistors on the head PCB (Figure 5). Since the PDC is a CMOS digital device, the power consumption is a function of the input rate. The three dynamic power contributions are: the pixel events, the input clock and the data transmission rate. To produce different pixel event rates, the integrated 2D SPADs are exposed to different light count rates and the associated power consumption is measured. For the clock contribution, the PDC is designed to work with an intermittent clock to be sent only when required for the acquisition and the data transmission. The power consumption is measured by sending a clock to the PDCs in a frequency range from 125 kHz to 200 MHz with 100 MHz being the targeted operating frequency. The energy per clock cycle is then extracted. For data transmission, the power consumption is measured with the same frequencies for the digital output buffer. This single-ended CMOS buffer energy required per transition is then extracted.

4 Results

4.1 SPAD Characteristics

The 61 SPADs have a square shape of 34 µm with rounded corners for a photosensitive area of 1026 µm$^2$. The SPAD PDE is above 35% in the wavelength range of 440 nm to 580 nm with a peak of 40% at 560 nm, measured with a different readout at an excess voltage of 8 V. At room temperature, the DCR is between 0.95 cps/µm$^2$ and 2.9 cps/µm$^2$, or about 1000 cps to 3000 cps for a single SPAD at a SPAD excess voltage of 5 V. At the same excess voltage and temperature, the afterpulsing is <5% for a hold-off time of 0.5 µs. The SPTR for a single chain of CMOS SPAD at 5 V, quenching circuit and flag tree output ranges between 72 and 93 ps FWHM.

4.2 Flag Timing Resolution

The flag timing resolution has two main contributions: the jitter of the electronics (QC, buffers, routing) and the non-uniform routing between each pixel and the flag output. Since the pixel index that triggered is not outputted, the propagation delay cannot be corrected and is treated as timing imprecision.

To extract the electronic jitter, without the impact of the non-uniform routing during the characterization phase, each pixel is enabled one at a time. Hence, the measured electronic jitter for each pixel includes the contributions from the trigger tree buffers, the QC electronics, the flag tree
buffers and finally the PDC output buffer. The measured jitter for each pixel is illustrated in Figure 7 and the average jitter value is 7.7 ps RMS.

![Pixel Jitter Graph](https://example.com/image.png)

**Figure 7**: Per pixel jitter including the trigger tree, the QC electronics, the flag tree and the PDC output buffer. The average measured jitter over the whole array is 7.7 ps RMS.

For the delay non-uniformity, the average delay is extracted for each pixel. Figure 8 shows the simulated (a) and measured (b) flag propagation delay distribution for each pixel index of one of the 4 PDCs, including the trigger tree. The minimum, maximum and average delays for both simulation and measurements are shown in Table 1.

![Delay Distribution Graph](https://example.com/image.png)

**Figure 8**: Flag propagation delay distribution per pixel including the contribution of the trigger tree. In (a) is the simulation model and in (b) is the measurement results.
One can observe the similarities between the simulation and the measurements, for example the lower propagation delay on "Pixel Y index" between 30 and 50 and "Pixel X index" close to 0. Moreover, there is a 1.5 ns average delay difference for each pixel between the simulation and the measurements caused by the time propagation on the PCB (not considered in the simulation). By subtracting the propagation delay of the measured and the simulated value (taking the 1.5 ns delay into account), every pixel average delay is within ±100 ps of the simulated value and 90% of the pixels are within ±50 ps which shows a good accordance between the simulation and measurements.

A histogram of the propagation delay is presented in Figure 9a. The array-wide propagation delay variation has two main contributions: the flag OR-tree (16.7 ps RMS) and the trigger tree (81.9 ps RMS). The simulated array-wide timing non-uniformity is 96.2 ps RMS and the measured timing non-uniformity of the 4 PDCs ranges between 89 ps RMS and 93.6 ps RMS.

The trigger tree is a characterization structure and is not used in the final system once the readout is integrated with the array of 4096 3D SPADs. For this reason, this trigger tree was optimized last in the readout design flow with the remaining space within the pixel array. This leads to a trigger non-uniformity worst than the one of the flag OR-tree and hence deteriorates the global measured flag timing resolution.

Since the simulated and measured timing non-uniformity are similar at around 90 ps RMS
and both the normalized propagation delay distributions are similar, it gives much credibility to
the simulated digital model of the circuit, which does not include IR drops on the supply mesh.
Then, the real flag OR-tree contribution is estimated by subtracting the simulated contribution of
the trigger tree routing from the measurements. Figure 9b shows both the flag OR-tree from simu-
lation (16.7 ps RMS) and the estimated flag OR-tree non-uniformity ranging from 37 ps RMS and
42.1 ps RMS. This provides an estimation of the electronics contributions of the ASIC readout of
the future 3D PDC.

4.3 Comparison of the Outputs

An acquisition of the three combined outputs is presented in Figure 10. Each red pulse is a flag signal
which indicates that a pixel triggered. The short duration of the flag signal (10 ns) allows to count
multiple flags close to each other. The blue curve is the analog monitor through its readout on the
head PCB. Its amplitude is proportional to the number of triggered pixels. The analog readout has
a time constant of approximately 50 ns to filter the digital noise. The adjustable current amplitude
and the readout gain result in 35 mV per pixel. The pulse duration follows the hold-off period of
the SPAD and is here programmed to approximately 500 ns. The grey dots are the samples from
the digital sum and the result follows the shape of the analog monitor. A 30 ns sampling period has
been set by the controller. The time constant of the low-pass filter on the analog monitor readout
explains the lower slopes on the analog monitor signal compared to the digital sum.

![Figure 10: The three outputs of the PDC combined in the same plot. The flag signal is presented
in red with arbitrary units, each digital sum sample is presented by the grey dots (left axis) and the
analog monitor is in blue (right axis). The digital sum follows the analog output with the analog
monitor vertical axis adjusted to a gain of 35 mV per pixel. The low-pass filter on the readout slows
down the slope of the analog monitor.]

4.4 Coincidence Window Acquisition Scheme

As explained in subsection 2.4, the flag output can be both timestamped or used to implement the
coincidence scheme with multiple PDCs. The coincidence allows to read only desired events, re-
ducing power consumption and output bandwidth. For example, a coincidence can be implemented
to discriminate the dark count of the SPADs. In that case, only real photon events are transmitted to
the tile controller. Figure 11 demonstrates two typical scenarios. First on the left, the LED used as
a light source is activated (shown in black). Photons are detected (flag signal in red) by the array of 2 × 2 readout with internal SPADs. The coincidence window is set for 500 ns into the tile controller and a photon threshold of 3 is expected. At the end of the window, more than 3 photons are detected for the LED pulse. The acquisition signal is sent to the PDCs (green pulse). The digital sum is then transmitted from the PDCs to the controller with a result of 6 photons detected. The second part of Figure 11 shows a second event for which only two single-photons are detected. Since it does not exceed the expected threshold, these photons don’t trigger an acquisition and a sum transmission. This scheme reduces power consumption since no clock is sent from the tile controller for rejected events, as shown in subsection 4.6. The pulse on the analog monitor after the first acquisition comes from the data transmission which induces noise on the analog monitor. Since the data is transmitted after the acquisition, it does not impact the operation of the PDC.

**Figure 11**: The LED activation signal (black) starts the event. It generates multiple photons that are detected and signaled by the flag (red). The analog monitor rises as well. The threshold is exceeded in the controller so the acquisition signal (green) is sent to get a single sample. The digital sum (grey) follows the analog monitor. On the right half of the plot, single flags do not exceed the threshold in the controller which won’t read the digital sum for a low power operation.

### 4.5 Continuous Sampling Capabilities

To demonstrate the continuous sampling operating mode, the LED is used as the light source. Figure 12 shows the overlap of the analog monitor and the digital sum of the PDC. The acquisition signal from the controller (green) indicates the different sampling modes; the continuous line indicates the fast sampling and the pulses indicate the slow sampling. The flag is presented on the lower subplot for better clarity. Here, the beginning of the acquisition is triggered by the coincidence window scheme in the tile controller. This method ensures to acquire only real events with the downside of loosing the beginning of the acquisition. A second method is to continuously perform the acquisition, without loosing the beginning of the event. But the power consumption (section 4.6) is higher. Finally, a third method is to trigger the acquisition on each flag and continue after a coincidence is detected. On the other hand, if no coincidence is detected at the end of the coincidence window, the acquisition is stopped and the acquired data ignored. This option proposes a better compromise between power consumption and loss of data.
Figure 12: On the higher subplot, the LED activation signal (black) is shown. The acquisition signal from the controller (green) set the sampling mode of the PDC with 50 fast samples (continuous part of the signal, each 10 ns) and 50 slow samples (intermittent part of the signal, each 50 ns). The digital sum (grey dots) follows the analog monitor (blue). On the lower subplot, multiple flags (red) are shown at the beginning of the event, showing a higher photon density. When multiples hits arrive closer to each others than the flag pulse width, they appear as a single larger flag pulse.

4.6 Power Consumption

The power consumption of the PDC includes both a static and a dynamic power consumption. A total static power consumption of 65 \( \mu \)W was measured. The major part of this static consumption (93 \%) comes from the static current sources required to adjust the duration of the hold-off, recharge and flag periods. Next, there are three contributions to the dynamic power consumption: the rate of the pixel triggering, the activity related to the digital clock sent to the PDC and the output buffers for data transmission. All these contributions vary depending on the operating conditions of the PDC and the discussion will elaborate on these results with examples.

The first measured dynamic power consumption is associated with the quenching circuits triggering rate and the propagation of the flag signal through the H-tree. It follows a linear trend for count rates \( R_{\text{events}} \) below 5 Mcps resulting in an energy of 8.8 pJ per event (equation 4.1).

\[
P_{\text{events}} (W) = 8.8 \times 10^{-12} \ (J) \times R_{\text{events}} \ (cps)
\]  

(4.1)
The second portion of the dynamic power consumption is related to the digital clock. Another linear trend was extracted from the measurements at frequencies from 125 kHz to 200 MHz, yielding to 1.8 nJ of energy per clock cycle. For a continuous clock frequency of 100 MHz, it results in 180 mW. The contribution of each circuit is known from simulations and some clock gating techniques will reduce this number in a following revision of the readout. Moreover, the PDC readout operates with intermittent clock and the power is calculated using the equation 4.2. Section 5 presents some applications to define the rate of the acquisition ($R_{acq}$) and the number of clock cycles per acquisition ($N_{clock\ cycles/event}$). It is shown that the clock power consumption is very low.

$$P_{\text{clock}} (W) = 1.8 \times 10^{-9} (J) \times R_{acq} \times N_{\text{clock\ cycles/acq}}$$  \hspace{1cm} (4.2)$$

The last contribution of the dynamic power consumption is associated to the data transmission ($P_{buf}$). This consumption is dependant on the load driven by the output buffer of the PDC. When the PDC drives a PCB trace of approximately an inch long, an energy of 85 pJ per bit transmitted is measured. Since the rate of the data acquisition ($R_{acq}$) and the number of bits to transmit ($N_{\text{bits}/acq}$) depends on the application, examples of power consumption are presented in section 5, based on equation 4.3.

$$P_{\text{buf}} (W) = 85 \times 10^{-12} (J) \times R_{acq} \times N_{\text{bits}/acq}$$  \hspace{1cm} (4.3)$$

Finally, the total power consumption of the PDC is the sum of the different contributions: static, events, clock, buffer.

$$P_{\text{total}} = P_{\text{static}} + P_{\text{events}} + P_{\text{clock}} + P_{\text{buf}}$$  \hspace{1cm} (4.4)$$

5 Discussion

5.1 Power Consumption

To appreciate the total power consumption, two cases for particle physics experiments in noble liquid are presented. The first one will be in liquid xenon and the second will be in liquid argon with pulse shape discrimination over multiple PDCs. The calculations consider a full 3D SPAD array integrated in 3D over this CMOS readout ASIC with an active area of $5 \times 5 \text{ mm}^2$.

5.1.1 Liquid Xenon Experiment

For low light experiments, the dominant count rate is the DCR. The nEXO experiment [12] targets a DCR below 50 cps/mm$^2$ at 167 K. This yields to a PDC count rate of 1250 cps. The event dynamic consumption is calculated using equation 4.1 which result in 11.0 nW. For a case where there is no dark count filter algorithm on the tile controller, each dark count event would trigger an acquisition to read the digital sum. A single acquisition of the digital sum and its transmission to the tile controller require 30 clock cycles. With 1.8 nJ per cycle, equation 4.2 results in 67.5 µW of dynamic power associated to the intermittent clock. To transmit the sum through the PDC output buffer, 20 clock
cycles are required. Equation 4.3 result in 2.1 µW. Finally, by adding the static consumption (section 4.6), a total power of approximately 140 µW per PDC is obtained (equation 4.4) or 560 µW/cm².

On a 4 m² experiment, the 160 000 required PDCs would consume 22.4 W of the 100 W budget for the light readout [12]. Moreover, if considering very low light events distributed uniformly over the 4 m², the probability of getting more than 1 photon per PDC would be very low [12]. Then, the tile controller could simply count the flags of each PDC without sending any clock to the PDCs. This would result in a power consumption per PDC of approximately 65 µW/PDC ($P_{\text{events}} + P_{\text{static}}$) and 10 W over 4 m².

5.1.2 Liquid Argon Experiment with Pulse Shape Discrimination

Since the temperature of the liquid argon (85 K) is colder than the liquid xenon, the DCR of a typical SPAD will be lower. Taking Darkside-20k experiment as an example [13], the DCR they measured at 77 K from FBK SiPM is 0.5 cps/mm². A PDC would then have a DCR of 12.5 cps. With equation 4.1, the event related power is 110 pW. If using the continuous sampling feature of the PDC with 20 samples each 10 ns (fast) and 50 samples each 200 ns (slow), it would be possible to measure the scintillation of the liquid argon over 10 µs. Equation 5.1 gives the number of clock cycles required for such an acquisition ($N_{\text{clock cycles}}$). First, the fast acquisition occurs for $N_{\text{fast}}$ clock cycles without any data transmission. Then, during the slow acquisition, the PDC transmits the samples using 20 bits per sample ($N_{\text{bits/sample}}$). Since the period of the slow samples (50) is greater than the transmission period (20), the PDC transmits both the fast and slow samples during the time of the slow acquisition. In total, the PDC needs 1420 clock cycles to complete the acquisition and transmission.

$$N_{\text{clock cycles}} = N_{\text{fast}} + (N_{\text{fast}} + N_{\text{slow}}) \times N_{\text{bits/sample}}$$

$$= 20 \text{ fast} + (20 \text{ fast} + 50 \text{ slow}) \times 20 \frac{\text{cycles}}{\text{sample}}$$

(5.1)

Then with equation 4.2, by using the event rate of 12.5 cps and 1420 clock cycles, the power contribution of this intermittent clock is 32 µW. Regarding the output buffer power (equation 4.3), 1400 bits are required ((20 + 50) × 20) per acquisition, hence leading to 1.5 µW. By summing the dynamic and the static consumption (equation 4.4), the total power per PDC in liquid argon is less than 100 µW or 400 µW/cm².

This result is lower than the 140 µW of the LXe case even if more samples are taken on each event. The explanation comes from the event rate that is much lower showing that the power consumption is a function of the input event rate. Low light means very low-power consumption. By using Darkside-20k as an example, the photosensing area would be 14 m² covered by 560 000 PDCs for a total of 56 W.

5.2 System Integration

The PDC readout presented in this paper is advantageous for its timing capabilities and the flexibility of its three output architecture. It is meant to replace the typical SiPM analog chain (SiPM module, preamp, shaper, ADC) in some experiments with the benefit of having novel embedded features as
well as a low-power consumption. A single $5 \times 5 \text{mm}^2$ PDC is not enough to cover the required area of multiple square meters for particle experiments: it has to be integrated into a larger system. Efforts are made to create SiPM tiles in a range from $5 \times 5 \text{cm}^2$ to $10 \times 10 \text{cm}^2$. This photodetection tile will need to integrate multiple PDCs.

The design of the PDC head test PCB (Figure 5) already requires a lot of components only for a $2 \times 2$ mini tile. From the 32 CMOS IO pads presented in Figure 1, 10 are digital signals used for configuration, acquisition control and data transmission. The others are optional analog test signals and redundant supplies and their current returns. When scaling up the number of PDCs to N on a tile, a controller might need $10 \times N$ IO pads. As an example, a tile with $5 \times 5 \text{cm}^2$ of photosensitive area would require 100 PDCs, hence a controller with at least 1000 IO pads. Another solution would be to include some fanout buffers on the tile to share hence reduce the number of IOs on the tile controller, but it adds more components in the system like in the head PCB design. The chosen solution is to produce a second revision of the 3D PDC readout that requires less individual IOs and opt for techniques like daisy chains with loop back. As well, even if the power consumption is already very low, more efforts will be made to reduce it using clock gating for high count rate applications.

6 conclusion

This paper presents the architecture of a novel 3D PDC readout to replace an analog SiPM readout chain. Designed to receive a $5 \times 5 \text{mm}^2$ array of 4096 3D SPADs, the readout includes the bonding pads to interconnect each SPAD to a CMOS quenching circuit. The output of each pixel is combined in three different outputs: an analog monitor, a flag to send to an external TDC or coincidence engine and a digital sum to get the precise number of pixels triggered. The readout also includes a row of 61 2D CMOS SPADs for validation prior to the 3D bonding of the final SPADs. This electronic is tested on a mini-tile setup of $2 \times 2$ PDCs. A SPTR ranging from 72 to 93 ps FWHM has been measured on 4 different PDC readout for the internal SPADs. The flag output timing resolution has been measured using an internal trigger tree. With both the contributions of the optimized flag H-tree and unoptimized trigger tree, this propagation delay impact on the timing resolution is below 95 ps RMS. With the 3D bonded SPADs hence no trigger tree, the estimated result would be below 45 ps RMS. The digital sum operation has been demonstrated and compared with the flag and analog monitor outputs for two modes of operation: a single sample based on multiple PDC coincidence and a continuous sampling to achieve pulse shape discrimination of the measured scintillation light. A power consumption below 140 μW per PDC can be achieved for liquid xenon experiment and below 100 μW for pulse shape discrimination in liquid argon. While some improvements are required for the large-scale system integration, the device is promising for light instrumentation as a replacement for analog SiPM.

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