A comprehensive review and side channel attack analysis on radiation-tolerant SRAM cells for aerospace, terrestrial and nuclear applications

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Abstract

In memory, single event upset (SEU) and single event multiple node upset (SEMNU) have become the principal problems during the past four decades. Significant dependability issues arise from these upsets in a variety of applications such as space, terrestrial, military, and healthcare sector. The use of scaled on-chip memory devices to store private and sensitive data has grown dramatically in the last several years across all the sectors. Memory devices are seriously at risk from non-invasive side-channel assaults (SCAs), which extract secret and sensitive information as well as during SEU/SEMNU, which may flip stored secret and sensitive information. This article presents the history behind the emergence of radiation-hardened circuits and survey of several techniques to mitigate the impact of radiation over the past few decades along with SCA based on leakage power analysis. By educating the researchers on two crucial on-chip memory issues—radiation effect SEU/SEMNU and SCA—this work seeks to accelerate co-design efforts.

Keywords

SEU, SEMNU, on-chip, SCAs, radiation-hardened circuits, leakage power analysis.
1 | INTRODUCTION

In order to improve the reliability against radiation and security of a system against theft that makes human life easier, the aerospace industry has provided with several amenities in the fields of satellite communications, tracking systems, military surveillance, etc [1]. In advanced nanometer technology nodes, SRAM designs, widely used in the aerospace industry, has been the centre of attraction to the highly energetic particles under the influence of harsh radiation environments leading to soft-error. The SRAM based memory array occupies a larger portion of the memory and constitute the largest area of the chip, contributing significantly to the leakage as well as dynamic power dissipation in the entire system, and hence, it plays an important role in processor optimization in terms of power, area as well as speed [2]. The area, power consumed by the circuit and speed has an important impact on the overall chip performance. Thus, to achieve a processor with faster processing speed, the design of cache memory with minimum area, lesser consumption of power, high-optimized speed and high and improved soft error protected cell is necessary. It is a challenging task to design SRAM cells for aerospace applications since space provides a much more hostile environment for SRAM cells. In the outer orbit, due to poor geomagnetic field, it leads to a greater impact of radiation and also produces highly energetic charged particles such as alpha particles (range of 4MeV – 9MeV), high-energy neutrons (>1 MeV) and secondary radiated particles induced from the interaction of “cosmic ray neutrons and boron” [3,4]. Typically, earth’s atmosphere absorbs the particles. A very small percentage of the particles travel through the atmosphere with sun being the biggest source of radiation. As the device moves farther away from the earth’s surface, there are more bombardment of cosmic rays. When these devices are placed closer to the earth’s atmosphere, less amount of radiation takes place. The earth’s atmosphere filters out a lot of radiation and only some particles that emerges are known as neutrons and alpha particles. However, for an electronic system in terms of reliability, the stability of SRAM cells in space made them an important element and hence, it is widely used [5]. Space applications like satellites, space stations are prone to heavy radiation (high-energy particles), which interfere with the semiconductor based electronic circuitry. The interaction of such radiation with semiconductors will have negative effects on circuit performances, which increases the probability of bit error rate. Therefore, the need arises to make the circuits tolerant to radiation, this process is known as radiation hardening. Radiation-Hardened by Design (RHBD) is defined as a method that makes the circuit tolerant to radiation by incorporating a mechanism into the circuit. Radiation Hardening is achieved by Shielding and adding Redundancy to the circuits [6]. Modification done for the standard SRAM design at the circuitry level is required, so that it can be more hardened from radiation in order to provide immunity from upsets occurring at a single event (SEUs) as well upsets occurring at multiple nodes (SEMNUs) at the same time, since these two are the major challenges resulting from high energy particles.

Over the last few decades, the use of memory devices that helps in storing secret and sensitive data has grown significantly in several applications. The system on chips and embedded memories are mostly constructed with SRAM array structures that dominate in terms of area and power, thereby making a major component in various cryptographic systems that includes electromagnetic cards, mobile devices and cryptography algorithms employed by wireless networks that stores information code and data [7,8]. In order to overcome this type of malicious assault, most of the security based techniques such as symmetrical as well as asymmetrical key-based cryptography are dependent on long and unpredictable secret key, but these approaches of safeguarding the systems makes realization goals difficult and expensive [9]. The attacker attacks the memory systems using software and physical approaches that is able to read the confidential data successfully. Hence, at the time of execution, the digital platforms (such as combinational or sequential or memory systems) are targeted by side channel attacks.

Radiation impacts on CMOS circuits can be roughly classified into three types: total ionising dose (TID), single event effect (SEE), and displacement damage (DD) [10]. Total ionising dose is when high energy particles produced by radiation, when enters electronic devices will produce electron-hole pairs, holes being less mobile than electrons get trapped in gate oxides, the accumulated positive charge will degrade the performance. Single event effects take place when, in a split second, high-energy particles impact the nodes of a device, changing the node voltage as well as disrupting data in memory and flip-flops. Displacement damage are those in which high energy particles when impacted on a device will collide with silicon atoms.
in the crystal lattice and displaces the atom from its position, this will increase the leakage current thereby degrading the performance of the device. The main sources of Radiation in Space are Van Allen belts, where the magnetic fields trap the radiation, Solar flares, and Cosmic Rays [11]. Furthermore ionization can be of two types: Direct ionization and indirect ionization. Direct ionization consists of the following: i) Alpha, Beta particles, ii) Heavy ions (LET; MeV. cm$^2$/mg) and iii) Low energy protons (>30 MeV). On the other hand, indirect ionization consists of the following: i) Neutrons, ii) Protons (>30 MeV) and Gamma Rays, X-Rays. Neutrons and high energy protons interact with Si nuclei to release secondary ionizing particles (up to an LET of 14).

Memory Circuits are further prone to Single Event Effect. Single Event Effects are the major threats faced by SRAM cells in memory circuits. Due to soft errors resulting from the impact of highly energized particles, the regular operation of the conventional SRAM cell gets affected such that the stored data gets reset when a highly energized ion strikes the cell, resulting in a failure of data and this anomaly is termed as a Single Event Upset (SEU) [12]. Single Event Effects (SEE) are categorized into two types: non-destructive and destructive [13]. The classification of SEE is shown in Fig. 1. Non – destructive single event effects are those type of single event effects that changes the node voltages of semiconductor device but do not lead to functional failure of device, whereas destructive single event effects are the type of single event effects that changes the state of the circuit that leads to the functional failure. Single Event Upsets (SEU) causes the node voltage of an SRAM cell or a latch to change, which causes the bit flip in the circuit, thereby causing a soft error. Single-event upset (SEU) is defined as a soft-error and non-destructive form of single-event effects (SEEs). An SEU takes place whenever a particle strike happens at the storage node. These particle strikes occur at the nodes of the SRAM cell, which are sensitive to radiation. A sensitive node refers to a node which is connected to an OFF NMOS/PMOS transistor at the drain terminal. This node will act as a collection point of charges due to particle strike. As the charge increases at the node, the voltage value shifts, which will further shift the bit value stored in the circuit. In a semiconductor device, the sensitive region is defined as the strong reverse-biased drain diffusion region where transient current induced in the device passes from the diffusion region of N – channel at the drain end to the P – channel diffusion region. Hence, a transient pulse, which is positive, gets induced when the radiation ion strikes the PMOS transistor drain and similarly, transient pulse which is negative gets formed when the radiation ion strikes the NMOS transistor drain.

The SEU can also be termed as soft error because the data altered by a single event upset caused by radiation particle is temporary in nature because the wrong data in the node affected gets changed with the appropriate data in the next write operation. In other words, since these corrupted data can be recovered fully by overwriting the state of operations, hence, such a phenomenon can be reported as soft error. Thus, it results in a system malfunction but it does not cause permanent damage [14].
This paper is presented as follows: Section 2 includes the background that covers the history of single event upsets and the emergence of SEE. Section 3 includes the impact of energetic radiation particles on SRAM circuits that leads to SEU and MEU and also related to its occurrence. Section 4 includes the occurrence and impact of SCA (side-channel attack) on SRAM circuits. Section 5 shows the modelling of critical charge and type of models proposed by the researchers for SEU tolerance analysis. Section 6 reviews various existing radiation-hardened by design (RHBD) SRAM cells. Section 7 includes comparison of design parameters for the reviewed RHBD SRAM circuits. Finally section 8 provides the conclusion.

2 | BACKGROUND
ICs which get fabricated especially digital CMOS ICs faces severe reliability issues when put in the vicinity of the radiation surroundings. In 1974, particle fluxes comprising of alpha particles and neutrons emanating from the radioactive elements first came into view outside the space environment. In 1975, Binder et al. reported in its statement that unexpected occurrence observed in communication satellite operators were caused as a result of sudden triggering of digital circuits [15]. Towards the end of 1970, the researchers came to the conclusion that soft error that took place in the satellite storage carrying integrated circuits were caused by the radiation particles in space. C. S. Guenzer in his study along with his partner introduced the term Single Event Upset (SEU) for the very first time [16]. After 1978, SEEs came into focus by the researchers as it was used to describe an upset caused by direct and indirect impact ionization.

In 1979, it was announced by two teams that the involvement of both protons as well as electrons could be responsible for indirect ionization that can result in the occurrence of SEU in digital ICs [16, 17]. In space environment, since protons are abundant in number compared to other particles, hence, the proton acts as a primary source for SEU. Subsequently, the researchers also came to the conclusion that SEUs are not only caused by the cosmic radiation, but also can be impacted by the presence of solar wind as well as protons captured in the earth’s radiation belt region. In the same year, for the first time Single-Event Latch-up problem has also been discovered by the researchers caused in the integrated circuits [18]. During this time, May et.al (1979) stated that some additional charge produced by alpha particles due to radiation accumulates in the reverse bias drain diffusion region of the MOS transistor resulting in bit-flip of the MOS device.

Towards the early 1980s, SEU became a serious research topic in the radiation-effect scientific community. The primary research during that period was mostly focussed on Dynamic RAMs, SRAMs and their involvement with latches and flip-flops [19, 20]. During the late 1980s, studies based on SEEs has been done in complex logic circuits [20, 21, 22]. Peterson et al. introduced the concept of the SEE on the memory devices which are caused by highly energized charged particles in space and terrestrial environments and this SEE can be further classified as SEL, SEU and SEB as shown in Fig. 1.

During the 1990s, the researchers in their quest to further harden the ICs against the impact of SEEs, were driven by two motivating factors. The first being that as the ICs complexity rate are increasing, larger number of circuits needs to be protected from the impact of radiation. The second being that as the silicon technology are being scaled down to incorporate a larger number of transistors, the feature size as a result was also decreasing. Hence this results in ICs being more vulnerable to SEEs. Towards the end of 1990s, it became more evident that errors resulting from SETs were more prominent in digital circuits, because the rate of SET in logic circuits get increased with clock frequency, while the SEU remains constant in charge storage cells. Now, in the twenty-first century, the rate of soft error has increased dramatically in memories, sequential circuits, and in combinational circuits as a result of device size scaling, decrease in power supply voltage and higher clock frequency. This causes a great threat not only to the electronics community in aerospace applications, but also can impact commercial products at the ground level. Hence, the fault tolerant function has become the main feature to fill the gap of reliability in the VLSI industry. Numerous radiation-hardened by design (RHBD) techniques have been incorporated in this research field. Some processes involving Silicon on Insulator that can minimize soft errors also been employed in the community [23, 24].

3 | IMPACT OF RADIATION PARTICLES ON SRAM CIRCUITS

When the radiation particles strike a logic circuit like SRAM, electron and hole pairs gets generated by impact ionization, i.e., the particles will be ionized as it loses energy. The presence of electron and hole pairs in the semiconductor gets separated due to the presence of electric field and hence are accumulated at the sensitive node as shown in Fig. 3. These excessive charges produced will be collected by the device nodes which are sensitive [13]. Due to this, a perturbation in voltage appears at those nodes. These charges once accumulated create both positive and negative transient voltage pulses. When the amplitude of these pulses overcomes the switching threshold that affects the memory circuit at the drain end of the inverter, the data which was originally stored gets changed, that results in an upset at single event (SEU) or soft error
as presented in Fig. 3. Fig. 4 depicts the positioning of current polarity of an inverter required to generate positive transient pulse if radiation strikes the drain end of PMOS and to generate negative transient pulse if radiation strikes the drain end of NMOS.

FIGURE. 3. Mechanism for generation of transient at device level when highly energetic radiation particles strike the PMOS of an inverter in integrated circuits
As we know, in today's era of digital world, the speed, power and area are the motivating factors for VLSI circuits development and hence, to bring an improvement in these factors, the CMOS circuits are being scaled down. Due to the continuous scaling in technology in the nanometre regime, the node capacitance of such cells has reduced considerably, thereby, increasing the vulnerability of the nodes to soft-error [25]. Hence, as technology scales down, SRAM cells are mostly affected by the impact of radiation considering the operation in the radiation environment. Moreover, as the distance between the transistors gets reduced significantly due to scaling, it results in charge sharing effect, and as a result, a single particle strike may result in a single-event multiple-node upset (SENU), which has become the major effect of energetic particles in emerging complementary MOS technology. This may lead to a single-bit upset if the nodes consisting of the same cell are present or a multi-bit upset if the nodes consisting of different cells are present. Hence, a greater number of transistors, more than one, are also vulnerable to the deposited charge resulting from a single particle strike in comparison to what is observed in previous older process where only one transistor was getting impacted. Among several memory cells, the SRAM cells have more chances of SEUs due to the presence of lower nodal capacitance and higher sensitive volume with increasing current densities. Therefore, there is an increase in the rate of soft error generation with scaling of CMOS technology in the nanometre regime. The susceptibility of the circuits further increases to radiation with the reduction or scaling in supply voltage and also decreases the critical charge. That is why, the development of radiation-hardened technologies in digital circuits, especially in memory circuits is very important.

4 | SIDE-CHANNEL ATTACK ANALYSIS ON SRAM CIRCUITS

With the constant scaling in technology, when we move below 100nm technology node, leakage becomes a primary energy consumer. Due to this reason, leakage power analysis (LPA) has emerged as a major cause of concern for the data security of cryptographic systems since the attacker exploits the correlation of the instantaneous power consumed by the memory and the processed and stored data of the memory [9, 26].
Leakage power attack analysis falls under the category of side-channel attack that the attackers exploit. The attackers can extract the information about the processed data or the cryptographic information that takes place. The radiation-hardened SRAM devices working in space environment is a major cause of concern as far as security is concerned because the attackers are able to exploit unwanted leakage information when memory performs its operation. Hence, making the SRAM security protected is of utmost importance.

The side-channel attack takes place due to the significant difference in the SRAM cell leakage current components when BL gets charged to write-’0’ and write-’1’ operation respectively. Hence, it depends on the number of subthreshold leakage current component in standby mode and the width of the transistors. The essential setup to measure the leakage power in standby mode is shown in Fig. 5, in which three different cases are being considered. The initial condition is to pre-charge both the bit-lines to V_{DD} and vary the data stored in the memory cell, while the next two cases are for “0”-storing state (write-0 operation) and “1”-storing state (write-1 operation) respectively.

Overall, the attacker is able to attack the memory blocks that contains information such as unequal leakage current components and unequal leakage weights through I_{sub-Leakage} that flows in the memory cell. The attacker is able to collect the data stored in the memory by collecting the leakage power samples as initially, the leakage power components are different for cases when Q stores “0” and “1”. If the leakage current of the cell having logic state “0” is less than that of having logic state “1”, then the attacker guesses that the storage node is storing logic state “0”, and if the key is not correct, then the attacker complements the key coming from the memory [9]. Thus, the only way to stop the attacker from performing SCA is to equalize the number of transistors through which subthreshold leakage current flows and also having equal widths or equal size of the transistors in case of memory storing different binary logic states. It is assumed that the attacker before extracting confidential information is already aware of the following conditions:

- Knowledge of the array or system architecture and thereby, has access to the power supply lines along with timing information of the system.
- Information related to memory organization from the memory architecture including peripheral circuits and internal timing paths of the system.
- Lower signal to switching ratio in order to remove the algorithmic noise from the total power components using enough current traces.

(a) (b) (c)

**FIGURE 5.** Condition to measure leakage power in standby mode during. (a) bit-lines pre-charged to V_{DD} and Q is varied. (b) write-’0’ condition. (c) write-’1’ condition.

5 | CRITICAL CHARGE MODELING IN MEMORY DEVICES

Critical charge plays a very important role in determining the SEU tolerance of the radiation-hardened circuit and to maintain its stability when the cell is impacted by radiation. Critical charge (Q_{crit}) is the minimum amount of charge accumulated at a sensitive node that can flip the stored data or change the storage state of the circuit. The lowest value of Q_{crit} among all the sensitive nodes gives the effective Q_{crit} of the cell. A radiation-hardened circuit should be able to restore its data after the impact of radiation that causes the node voltage to change and gives incorrect data. The radiation can strike possibly every node of the cell but only the sensitive node will get affected from radiation strike that causes change in data. The
radiation can strike and impact a single sensitive node or it can strike at dual or multiple sensitive nodes at the same time that causes bit-flip of both the nodes simultaneously.

Hence, to simulate the impact of radiation across those nodes of a radiation-hardened cell, a double exponential current pulse model is being applied across the sensitive nodes of the cell to verify SEU and DNU and also to calculate the critical charge. When the radiation particles strikes the drain terminal of an OFF NMOS transistor, a double exponential current source is applied that produces negative transient pulse since negative charges gets accumulated across the drain node (10 SEU). Similarly, when radiation strikes the drain terminal of an OFF PMOS transistor, a double exponential current source is applied, such that it produces positive transient pulse since positive charges gets accumulated across the drain node (01 SEU). Whenever these amount of positive and negative charges accumulated by the particle striking the sensitive node is greater/larger than the critical charge \( Q_{\text{crit}} \), which is the least amount of charge required to alter the stored logic state of the memory cell, the SEU and DNU will take place.

The negative and positive transient pulse depends on the polarity of the current source applied. In case of NMOS, the direction of the current should be away from the drain end of OFF NMOS and towards the ground terminal whereas, in case of PMOS, the direction of the current source should be towards the drain end of OFF PMOS as shown in Fig. 4. If more than one node gets impacted from radiation, then multiple current sources are applied across the sensitive nodes at the same time by following the similar topology to mimic the effects of multiple strike and charge sharing. The dual node upset recovery has been considered under the case that two sensitive nodes with different potential are disrupted by the impact of radiation.

In the literature, there are four models used for the estimation of the SEU tolerance or to characterize \( Q_{\text{crit}} \):

1. Simplified model by Roche
2. Current model by Freeman
3. Diffusion collection model
4. Double exponential current model

The Space electronics community generally uses TCAD tools in 3D device simulation environment for critical charge characterization as well as soft error estimation, whereas the circuit community uses SPICE - level current models for \( Q_{\text{crit}} \) estimation.

However, the circuit community prefers double exponential current model more since the waveform shape and the current amplitude of the current exponential model have a strong impact on the computation of critical charge.

The equation for the double exponential current model is given as,

\[
I(t) = I_0 \times \left\{ e^{-t/t_\alpha} - e^{-t/t_\beta} \right\}
\]

(Equation (1) provides the current injected at the node) \( I_{\text{peak}} = \frac{Q_{\text{inj}}}{(t_\alpha - t_\beta)} \)

(Equation (2) provides the charge collected at the sensitive node)
where, $I_o$ is the amplitude of current pulse, $Q_{coll}$ is the amount of collected charge generated by high-energy particle collision.

![FIGURE 6: SEU Recovery Waveform for Node Q of 6T SRAM cell](image)

While estimating the critical charge, the state of the cell is in hold mode. The access transistors are excluded for critical charge analysis due to the un-accessed or retention mode of the cell when a particle strikes.

Here, we measure the critical charge at the sensitive node that gets affected by radiation. In conventional 6T SRAM cell, the node Q can be impacted by the radiation particle strike due to the OFF NMOS N1. So, to measure the critical charge, a current pulse is placed across the terminal of the node Q. The simulation performed in 65-nm technology is shown in Fig. 6 for SEU recovery. Similarly, the radiation particle can strike the drain region of an OFF PMOS P2 of the conventional 6T SRAM cell. However, the conventional 6T SRAM cell fails to capture the essence of radiation-hardened SRAM cells. Generally, for critical charge calculation, we are considering hold mode in which the word line signal gets deactivated and the access transistors are turned OFF, thereby disconnecting the BL and BLB to the storage nodes. Here, the critical charge is characterized by using double exponential current model technique.

Even though 3D TCAD used in other models can fetch a good accuracy level, but at the same time, also suffers from huge computation times along with restricted capabilities to simulate circuits that exceeds relatively smaller sizes. The 3D device and mixed-mode simulations are computation intensive and requires a fairly long development and calibration phase compared to the SPICE-type circuit simulation. Thus, it is desired to model radiation strikes as current sources that can be injected easily for faster SPICE simulations.

The current pulse rises as well as fall times along with their full-width at half-maximum (FWHM) strongly affect the $Q_{crit}$ characterization to a point where each pulse model results in its own $Q_{crit}$ value.

According to Roche, $Q_{crit}$ can be found by using the equation:

$$Q_{crit} = C_N V_{DD} + I_{DP} T_F$$ (3)

where, $C_N$ is the node capacitance of the circuit, $V_{DD}$ is the power supply, $I_{DP}$ is the maximum drain conduction current of the PMOS (the ion strikes at the drain of an OFF NMOS) and $T_F$ is the flipping time of the cell. The parameter $T_F$ is computed by using 3D device simulation in which the transient voltage of the opposite node (not struck by radiation ion) in the cell is observed during the period in which the cell flips its state. If we consider SPICE simulations, then the term $I_{DP} T_F$ can be ignored from equation (3) and $Q_{crit}$ can be found by integrating and exponentially decaying current ($I_o e^{-t}$) with small time constants less than 20ps.
Hence, we strongly prefer the double exponential current mode to estimate the critical charge ($Q_{\text{crit}}$) due to its accuracy.

6 | REVIEW OF STATE-OF-THE-ART RHBD SRAM CELLS

The design can be classified into five categories based on reliability. The first category represents the SRAM cells that is not able to recover from SNU, but consists of simplest structure and provides low average power consumption or exhibits lowest power consumption. The second category represents the RHBD cells that can recover from SEU partially and has a relatively simple structure. In this type of designs, not every nodes are fully recoverable from radiation impact. The third category represents the RHBD cells that can tolerate SNU as well as DNU partially. These design has sensitive nodes that can recover from single strike radiation effects but cannot recover from DNU fully. The fourth category represents those RHBD cells that can completely achieve SNU as well as DNU recovery. In these designs, all the node-pairs are recoverable from DNU effects. The fifth category represents the category of SRAM cells that are protected from side channel attacks but are not radiation hardened and contains only two charge storage nodes apart from RHLR12T which is both radiation hardened and also leakage power attack resilient.

6.1 | FIRST CATEGORY OF REVIEWED SRAM CELLS

6.1.1 | Conventional 6T SRAM Design

The six transistor SRAM cells, possessing positive feedback, does not have enough capability to handle SEUs since a change in voltage (due to the impact of radiation strike) in one node causes the other node voltage to flip its state due to its feedback mechanism [13]. Hence, the conventional 6T SRAM cell is not able to provide sufficient reliability in the outer environment of space containing radiation. The design also possess a lower power consumption due to its smaller transistor count, thereby having a less area.

6.1.2 | 7T SRAM Cell Design

G. Surekha et al., designed a 7T SRAM cell [28], consisting of seven transistors and two storage nodes. The design is a modified version of the basic six transistor SRAM cell by connecting a NMOS transistor to the source of both the pull-up PMOS transistors. The extra NMOS transistor is connected with the supply voltage and its gate terminal is connected to the word line. The design has been able to improve the static noise margin during hold, read and write mode and also the power consumption has been reduced considerably compared to the conventional 6T SRAM cell. However, the design fails to recover from radiation upset and is not resistant to SEU.

6.1.3 | Schmitt trigger-based 8T SRAM Cell Design

T. Vasudeva Reddy et al., designed a Schmitt trigger-based eight transistor SRAM cell [29], in which a 256 bit cell has been proposed consisting of 256 single Schmitt trigger-based 8T cell. The design consists of eight transistor for a single bit cell out of which the pull-down transistors are stacked to one another. The design has been able to achieve low power dissipation compared to the previous designs, but, these designs are mostly focussed on reducing power consumption, delay and noise margin and not radiation resistant. Hence, designing radiation hardened memory cell is not only used for the harsh space environment, but also for nuclear environment, and as a result, it becomes increasingly necessary to make the memory design such as these tolerant to high energy particle strike. The next category will discuss about the existing RHBD cells that has radiation hardening tolerance.

6.2 | SECOND CATEGORY OF REVIEWED RHBD SRAM CELLS

6.2.1 | QUATRO -10T, WE-QUATRO designs (Year: December 2009; September 2017)

In [30], Jahinuzzaman et al. proposed a quadruple 10 transistor radiation tolerant robust SRAM cell, QUATRO-10T that provides differential read operation and exhibits larger SNM and less leakage current. QUATRO-10T is capable of recovering from SEUs produced at the “1” storing storage as well as internal nodes and also at “0” storing internal node but the design cannot recover from SEUs induced at the “0” storing storage node. Thus, QUATRO-10T is capable of reducing only logic “1” logic “0” upsets with the help of negative feedback mechanism. The “1”-storing (“0”-storing) main storage node are driven by PMOS P3 (NMOS N1) transistor. Similarly, the storing state - “1” (storing state - “0”) of the internal node is driven by PMOS P2 (NMOS N4) transistor respectively. The QUATRO-10T SRAM cell flips multiple nodes when impacted by radiation through charge sharing. Even though the target cell has been distanced as far as possible in order to reduce the possibility of multiple node upsets, still, this design has not been able to provide recovery from a single event multiple node upset (SEMNU). Thus, at least when two charge storage nodes are impacted by charged particles at the same time, this design cannot provide immunity to both the nodes. Due to the presence of dual interlocking and cross-coupling structure, it eventually leads to good soft-error resilience and helps the node in recovering to its earlier state after upsets occurring at a single event. Hence, for utmost reliability in the space environment, a cell with higher critical charge capable of tolerating soft error is considered as a better alternative for space applications. However, the design has write performance flaws considering the write margins and write access time. It contains large write delay and hence, its ability to write data is poor. The presence of double interlocking structure makes wiring complex while performing cell layout and leads to area penalty. When this design is injected by an alpha particle at minimal voltage, the design cannot be recovered because of its inherited differential read capability. To improve the write operation, an improved version of QUATRO-10T, named WE-QUATRO [33] has been proposed. However, the cell still faces the problem of high static and total power consumption with less
stability. Hence, WE-QUATRO has power and delay penalty. Moreover, WE-QUATRO cannot recover from SEMNU issues.

6.2.2 | NS-10T, PS-10T designs (Year: 2012)

In-Seok Jung., et al., proposed two novel SRAM cell designs [31] consisting of 10 transistors that provides higher SNM for low voltage application. This paper addresses the previous problem reported in QUATRO-10T which was unable to withstand the highly energized particle strike considering the case when the cell is operating at low voltage. Thus, this paper consisting of stacked PMOS (NMOS) transistor PS-10T (NS-10T) design helps to eliminate soft error in low operating voltage condition. This design is capable of withstanding the impact of SEMNU since a least possible distance between the charge storage nodes to the redundant (internal) node has been maintained by the author. SEMNU occurs due to charge sharing phenomenon since the transistors are kept at a very close distance to one another as a result of technology scaling. Using stacking effect, the design offers low supply voltage operation for dynamic voltage scaling technique. However, these designs provides partial immunity to SEUs. PS-10T is able to store “1” and can recover from “0” to “1” SEU (i.e., prevents “1””0” SEU) and NS-10T is able to store “0” and can recover from “1” to “0” (i.e., prevents “0””1” SEU). Hence, both the designs are not completely immune to SEU and is able to provide only partial recovery on the basis of upset polarity on a single node. In NS-10T, a stacked NMOS pull-down path is used resulting in a longer read delay. Nodes C along with D are driven by pull – up MP3 (to logic “1”) and pull-down MN3 (to logic “0”). In PS-10T, for “0”-storing state, C and D nodes are driven by pull-up MP2 (to logic “1”) and pull-down MN2 (to logic “0”) respectively.
(i) (ii) (iii) (iv)  
(v) (vi) (vii) (viii)

**FIGURE 8.** RHBD designs. (i) QUATRO-10T [30]. (ii) WE-QUATRO [33]. (iii) NS-10T [31]. (iv) PS-10T [31]. (v) RHD-12T [32]. (vi) QUCCE-10T [36]. (vii) QUCCE-12T [36]. (viii) CC14T [55].

### 6.2.3 | RHD-12T design (Year: July 2016)

Chunhua Qi et al., 2016 in [32] proposed a reliable cell design RHD-12T that contains four data storage nodes (Q, QN, S0 and S1) with 12 transistors. The cell is a modified version of QUATRO-10T design in which two PMOS transistor (P3, P4) has been added to the QUATRO-10T design. Additionally, the cell is also an enhanced version of stacked PMOS PS-10T design where two additional PMOS transistors (P1, P6) are added to PS-10T design. The design claims to provide recovery from an SEMNU produced at its internal node-pair, but it is unable to recover from an SEU induced at its “0”-storing storage node similar to the previous reported designs [30][31]. However, the use of stacked PMOS transistors results in parasitic bipolar amplification. Hence, the RHD-12T design uses source isolation technique while doing layout level simulation across the drain and source regions of P6 and P4 transistors respectively. However, it comes with a penalty of overall larger area. There is a need to improve the probability of failure, as it is partially tolerant to single event upset at multiple nodes. Moreover, the cell possesses slower write speed and a larger power consumption.

### 6.2.4 | QUCCE-10T, QUCCE-12T designs (Year: October 2018)

Jianwei et al., 2018 in [36] proposed two pairs of PMOS and NMOS cross coupled inverter latches (QUCCE-10T and QUCCE-12T) that forms four storage nodes consisting of ten transistors. Another design QUCCE-12T consists of the modified version of QUCCE-10T design that contains two additional NMOS access transistors N7 and N8. The two excess access transistors present in QUCCE-12T design connected to the internal node assist during the write operation and helps in WAT and write margin improvement of the design. QUCCE-12T have a considerably lower read access time due to the two discharging path present in the cell that activates during read 0 or read 1 operation. Hence, QUCCE-12T is able to achieve better read and write margins. Since a longer feedback loop is present in the design, the QUCCE-10T have larger WAT
when write operation takes place. The stacked NMOS structure present in the cell results in a decrease in the leakage power. QUCCE-12T suffers from larger area overhead and leakage power penalty due to the presence of higher dominated leakage path from BL/BLB to ground and from VDD to ground. Hence, the design results in a higher leakage power compared to other designs. QUCCE-10T suffers from larger WAT during write operation due to the presence of longer feedback loop. QUCCE-10T design also suffers from the charge sharing issue due to its direct cross-coupled connection to the storage nodes. The design is also affected by the single event multiple nodes upset. QUCCE-10T shows poor write ability and recover only from a 1 0 SEU. The design exhibits a lower critical charge ($Q_{\text{crit}}$) compared to the earlier designs. The QUCCE-12T design cannot provide immunity to SEMNU caused at the node-pair and cannot recover from a 0 1 SEU.

6.2.5 | CC14T design (Year: June 2023)

Nagma Sahi et al., 2023 in [55] designed a soft error tolerant SRAM cell consisting of fourteen transistors with four storage nodes along with four PMOS pull-up transistors, six NMOS pull-down transistors and four access transistors. The design takes more time to discharge during read operation due to the presence of stacked pull-down NMOS transistors, and hence, the read access time increases. The drawback of this design is that since it is surrounded by both PMOS and NMOS, hence the node-pairs increases. The probability of SEU strike is more due to more number of sensitive nodes and hence the SEU and DNU probability increases and sensitive area also increases.

6.3 | THIRD CATEGORY OF REVIEWED SRAM CELLS

6.3.1 | RHM-12T design (Year: February 2014)

Jing Guo et al., 2014 in [13] described a novel RHM-12T cell that overcomes the problem of single event upset as well as recovery from multi-node upset previously faced in QUATRO-10T, NS-10T and PS-10T. Two NMOS transistors are stacked above pull-down NMOS transistors that reduces the driving ability of pull-down NMOS transistors and also increases the read access time of the cell but lowers the write access time due to reduced driving capabilities at nodes Q and QN. Hence, due to excess transistor stacking, there is limitation in its supply voltage ($V_{\text{DD}}$) scaling. The storage node Q is being driven by a NMOS transistor resulting in a weak ‘0’. This weak ‘0’ reduces the driving capability of NMOS N4. The reduced driving capabilities at node Q and QN also leads to lower RSNM. Due to reduced feedback gain in RHM–12T, the HSNM is lower than that of PS-10T. RHM–12T, despite having a larger area overhead than most of the comparison cell, it has the least SEU probability occurrence because of lower sensitive area ($P_{S}$). It possesses much lower RSNM due to the presence of NMOS as pull-up devices. The RHM-12T cell faces the problem of large area and time penalty and low RSNM.
(i) (ii) (iii) (iv)

6.3.2 | RHBD-10T design (Year: May 2018)

Jing et al., 2018 in [34] proposed a radiation hardening by design (RHBD) 10T that uses upset physical mechanism merged with reasonable transistor sizing to enhance the reliability level of the cell. The design is a modified form of PS-10T as well as QUATRO-10T. The RHBD-10T design has PMOS transistor stacked...
instead of NMOS transistor to the QUATRO-10T design. The proposed cell uses transistor polarity mechanism and capacitance effect of the circuit, thereby, preventing the cell from any single-node upset. However, even though cell provides high radiation capability, but it does at the cost of write and read access times possessing more RAT. Moreover, since large number of PMOS transistors are present in the design, the parasitic bipolar effect existing in the PMOS transistors amplifies the probability of charge sharing between the circuit nodes especially that are sensitive. The design is able to recover from 1 to 0 and 0 to 1 bit in any node but it cannot provide recovery to an upset caused at node-pair. Hence, RHBD-10T design is unable to recover from SEMNU issue.

6.3.3 | RSP-14T design (Year: February 2018)

Chunyu Peng et al., 2019 in [35] presented an enhanced speed and power radiation-hardened design (RSP)-14T for space application. The design is a modified version of RHD-12T in []. The RSP-14T cell has added two additional PMOS transistors (P7, P8) to the previous RHD-12T design to limit the power consumed by the circuit during write operation. The RSP-14T design provides resemblance to the previous PS-10T design by incorporating PMOS transistors (P3, P6, P7, and P8) to the structure. The polarity hardening method has been used for RSP-14T design based on probability characteristics of single particle effect in order to reduce the node data upset probability. A source isolation technology has been used for RSP-14T cell. The source of four PMOS transistors (P3, P6, P7 and P8) are connected to the operating supply voltage.

Considering the state of the cell to be logic “1”, the quantity of drain charge stored by the transistor P2 gets weakened by the presence of stacked PMOS structure, which in turn, reduces the chances of SEU occurrence at node QB, thereby, making the cell more stable. However, if enough charge gets collected, it still cannot fully recover the data when the cell stores logic “0”, if it is flipped by an SEU. When the positive transient pulse strikes at Node QB, the voltage at node Q changes from logic “1” to logic “0” and remains at 0. Hence, this changes the data storage state of the cell and cannot return back to its initial state and shows partial immunity. Moreover, since all the charge-storage nodes along with internal nodes are surrounded by both NMOS and PMOS, it consists of six sensitive node-pairs for DNU analysis. Moreover, it provides poor read stability and has higher WAT compared to the previous designs. The read and write SNM of RSP-14T cell is also less compared to the previous mentioned designs, that results in reduction is the overall stability of the design. Hence, a different approach is required.

6.3.4 | RHPD-12T designs (Year: March 2020)

Qiang Zhao et al., 2020 in [37] proposed a novel radiation hardened by polar design (RHPD) design that increases reliability and enhances the operating speed of the design for space applications. The RHPD-12T design provides high radiation-hardened capability, high reliability, speed and good write ability by incorporating more NMOS transistors of larger width in order to provide enhanced robustness with good write ability. On the basis of providing recovery from all SNU, it can also recover from some DNUs to its previous state but it shows partial tolerance to single event multiple effect upset. The main drawback of this cell is read access time. Moreover, NMOS transistors N1 and N2 are connected to the $V_{DD}$ leading to lower driving capability. As a result, an alternative approach is required.

6.3.5 | RHBD-10T designs (Year: May 2020)

Govind Prasad et al., 2020 in [38] proposed a radiation hardening by design RHBD-10T design that is radiation hardened in nature and is able to increase the write ability (to increase the noise margin) of the cell. The RHBD design provides good soft error resilience, higher SNM, lower power consumption, moderate delay and lesser area occupancy. RHBD-10T provide better SEU resiliency, higher SNM, less leakage power consumption, lesser area and comparable delay. The presence of PMOS (P4, P5 and P7) in the pull-up path for Node A results in strong 1. The RHBD-10T cell contains more PMOSs (six PMOSs) with nominal size so that less total power can be achieved by the design. However, more PMOSs leads to an increase in parasitic bipolar amplification. Due to the symmetricity of the design, the data stored can be recovered whenever nodes A, B, C and D and node-pair B-C, A-D, A-B, C-D, A-C are upset by a radiation particle or charge sharing effect, but in case of node-pair B-D, the data cannot be recovered after upset. Thus, an alternative
approach is required for SEMNU recovery.

6.3.6 | RHBD-14T (Year: March 2021)

Naga Raghuram et al., 2021 in [39] proposed a radiation-hardened-by-design (RHBD) 14T that is claimed to have recovered from multi-node upsets. The RHBD-14T is made up with the use of four stacked inverters Inv1, Inv2, Inv3 and Inv4. The junctions between that of PMOS and NMOS devices of those inverters contains the nodes Q, QN, S0 and S1. The RHBD-14T has two sensitive nodes resulting in a decrease in $A_S$ (sensitive area) of the cell, thereby providing robust operation. However, it cannot provide recovery from a ‘1’ ‘0’ upset at a single event produced at its internal node. Also, it has a higher possibility of read upsets and displays poor stability during read operation due to the use of more PMOSs.

6.3.7 | RHMD-10T design (Year: June 2021)

Soumitra Pal et al., 2021 in [40] presented a soft error tolerant radiation hardened memory-by-design (RHMD-10T) cell that possess four storage nodes with ten transistors to mitigate SEU and SEMNU issues. The RHMD-10T design is a replicate of RHBD-10T design in which the author connected the PMOS transistors P1 and P2 to the redundant storage node S1 and S0, whereas, in RHBD-10T design, both PMOS P1 and P2 are connected directly to $V_{DD}$, and as a result, this design helps to mitigate SEU in all polarities. The design is capable of recovering from SEUs of both polarities induced at any sensitive node along with SEMNUs induced at one node-pair. RHMD-10T consumes lower $P_{Hold}$ (hold power) due to its stacking mechanism in the core inverter and PMOS P5 and P6 being used as the weak pull-down path. RHMD-10T provides good read stability due to its lower body effect, and also exhibits higher write ability. However, RHMD-10T shows a higher write failure probability. At lower supply voltages, the design has a higher WAT and also reduces the write margin of the design. Hence, the stability of the design is not suited for highly reliable aerospace applications.

6.3.8 | SEA-14T design (Year: August 2021)

Soumitra Pal et al., 2021 in [41] proposed SEA-14T (Soft-Error-Aware) cell consisting of four nodes that stores data charge storage nodes and 14 transistors that provides recovery not only from upsets occurring at a single event produced at any one sensitive node, but also for recovering from a multi-node upset produced at the internal node-pair. SEA-14T shows improvement in resilience against SEUs at every sensitive node regardless of strength and polarity. The SEA-14T cell is an updated version of RH-14T design, in which the author has two NMOS (N5 and N6) transistor added to the design and removed PMOS P7 transistor. SEA-14T consumes less leakage power due to the presence of excessive stacked transistors at both its outer branches as well as its inner core inverters as well. However, SEA-14T possesses a larger read and write delay due to the reduced driving capability of the node Q as it gets pulled up by an NMOS transistor. Thus, SEA-14T is more likely to have read upset, especially at lower voltage. As a result, the stability of the design is not as per the desired mark.

6.3.9 | SIRI design (Year: October 2021)

Authors in [42] proposed a novel soft-error-immune read-stability-improved (SIRI) SRAM cell consisting of four charge storage nodes including fourteen transistors that is capable of recovering to its initial state from SEUs as well as SEMNUs. All the sensitive nodes of the design are able to retrieve the data lost from SEU effect. The cell exhibits higher immunity against SEU across all its sensitive nodes and also possess higher read stability. The reliability of the design is more due to higher critical charge ($Q_{crit}$) than the previous mentioned designs. However, the design possess the drawback of increased read delay when applied at lower supply voltages. Thus, another approach is required.

6.3.10 | SAR-14T design (Year: June 2021)

Soumitra Pal et al., 2021 in [43] presented SAR-14T radiation-hardened SRAM cell that contains four nodes that stores data and 14 transistors to mitigate soft error issues. SAR-14T is a modified version of RHBD-12T SRAM cell. The SAR-14T design has two NMOS N5 and N6 added to the structure compared
to the RHBD-12T design. The design exhibits greater tolerance to SEUs produced at every nodes which are sensitive and also provides recovery from DNUs caused at its internal node-pair. The good feature of this design is higher critical charge ($Q_{\text{crit}}$) in comparison to the previous designs. Due to the presence of read-decoupled characteristics of SAR-14T, the design is free from read upset. The SAR-14T design uses a cross-coupling inverter connection structure, and four NMOS pass transistors that connects the nodes (both internal and storage nodes) with the bit-lines. SAR-14T used four NMOS pass transistors to write data into the cell, but only two NMOS pass transistors are used to read data. However, when sufficient charge gets collected at the charge storage node that stores “0”, the cell cannot provide immunity to SEU. Due to the addition of two access transistors N9 and N10, RAT increases which is the drawback of this design.

### 6.3.11 | LWS14T design (Year: December 2021)

Govind Prasad et.al., 2021 in [44] proposed a cost effective radiation tolerant soft-error aware-14T (LWS-14T) that is capable of recovering from upsets both occurring at single node as well as multiple nodes of the cell. LWS-14T possesses higher write speed since node B in LWS-14T cell is discharged faster due to weak logic “1” state, as it gets pulled up by NMOS N6. However, the read delay is higher since the access transistor(s) driving strength gets decreased as a result of adding two more access transistors (N7 and N8) to the design. In the design, since both the storage and internal node gets affected during read operation, it possess deteriorated read stability. The design has high energy consumption during both read and write operation due to its high dynamic power consumption.

### 6.3.12 | SIS10T design (Year: March 2022)

Soumitra pal et al., 2022 in [45] designed a Soft-Error-Immune (SIS10T) SRAM cell that includes four charge storage nodes and 10 transistors out of which two are PMOS transistors and eight are NMOS transistors, thereby, providing good tolerance from soft error with low area cost. The design exhibits good read as well as write performance even at extreme temperature conditions. SIS-10T exhibits high read stability, highest write ability and dissipates lower hold power. The read stability of the design gets diminished at higher temperatures. The design also shows improved RAT and WAT at lower supply voltages. SIS-10T dissipates lowest hold power due to the presence of two NMOS transistor for sinking current to ground terminal. SIS-10T contains a slightly longer read delay and shorter write delay in comparison to the conventional 6T SRAM cell because of reduced driving capability of N4 acting as pull-down transistor.
(i) (ii) (iii) (iv)

(v) (vi) (vii)
6.3.13 | SARP12T design (Year: March 2022)
Soumitra Pal et al., 2022 in [46] proposed a radiation resistant RSNM enhanced low-power soft-error-aware 12T (SARP12T) SRAM cell. The design is capable of regaining its original data produced at a single node or even multiple nodes even after the node voltages gets flipped by the charged particles. Furthermore, SARP-12T consumes the least hold power. All these improvements in SARP12T are obtained by exhibiting only a slightly longer read delay and consuming slightly higher read and write energy.

6.3.14 | NRHC-14T design (Year: November 2022)
Qiang Zhao et al., 2023 in [47] proposed a new radiation-hardened SRAM cell (NRHC-14T) is proposed that uses polarity hardening technique to reduce the sensitive node of the design and has the capability to recover from single-node upset as well as Dual-node upset produced at the sensitive nodes of the structure by radiation. However, it possesses two NMOS (N5 and N6) pass transistors and two additional PMOS (P7 and P8) pass transistors and provides good reading speed compared to those that contains only two NMOS access transistors, but it does not provide much higher reading speed when compared to cell that possess 4 NMOS access transistors.

6.3.15 | HPHS12T design (Year: January 2022)
Zhongyag et al., 2023 I [51] proposed a high stability soft error resistant (HPHS12T) consisting of 12 transistors based on polarity reversal strategy and stacking of NMOS and is capable of recovering not only from single event upsets but also from multiple node upsets. The design eliminates the problem of parasitic bipolar effect since only 2 PMOS transistors are used unlike in that uses extra PMOS transistors that provides higher parasitic bipolar amplification in comparison to that of NMOS transistor. However, since weak logic “1” and weak logic “0” nodes are present, it results in a larger static hold power consumption.

6.3.16 | RHBD-13T design (Year: April 2022)
Govind Prasad et al., 2022 in [49] published a radiation tolerant (RHBD-13T) SRAM cell design that uses unique feedback path mechanism among its internal nodes and has separate read as well as write circuitry, thereby, improving the operating speed of the design. The cell is capable of recovering from SNU’s as well as MNU’s caused by radiation strike. Since the design possess stacking effect and weak pull-down PMOSs, it consumes lesser leakage power. The cell design contains only one sensitive node for DNU analysis.

6.3.17 | RHD10T design (Year: July 2022)
Raghav Shekhar et al., 2022 in [50] designed a novel 10T radiation hardened by design (RHD10T) SRAM cell that provides energy-efficient operation with high noise margins, area efficiency and improved immunity of SEU. Upon comparison, RHD10T reduces the area overhead compared to QUCCE-10T and QUCCE-12T and also improves the HSNM/RSNM compared to RHPD-12T. Because of the leakage current present in the cell, the reliability of the RHD10T cell degrades considerably.

6.3.18 | RHMC-12T design (Year: Jan 2023)
Licai Hao et al., 2023 in [51] designed a radiation tolerant memory cell (RHMC-12T) that uses twelve transistors with four pull-up PMOS transistors and two pull-down NMOS transistors and contains two storage nodes and two internal nodes. The author used polar design strategy to mitigate soft error. The design consists of six node-pairs of which five node-pairs are vulnerable to DNU. However, among those five node-pairs, only three node-pairs can be recovered from DNU and the rest two node-pairs are not self-recoverable. Hence to avoid this, the author performed reasonable layout topology by keeping adequate spacing between the transistors (about 1.70 um and 1.85 um) for those two node pairs ((I1, I2) and (I2, I4)). This reasonable transistor spacing eliminates the possibility of charge sharing caused by DNU that results in data flip for these node-pairs simultaneously. The drawback of this design is that the design provides partial recovery to DNU and has to rely on layout topology for DNU mitigation for some of these node-pairs. The design also has a pull-down PMOS transistor that results in weak 0 across node I2.

6.3.19 | CC18T design (Year: February 2023)
Shuo Cai et al., 2023 in [52] designed a cross-coupled 18T SRAM cell that uses eighteen transistors and has four storage nodes. The design consists of two-input C-element structure and uses NMOS stacking mechanism so that the average power consumption can be reduced along with having feedback loop with the help of redundant transistors in order to improve reliability. The two-input C-element structure has been taken as a reliable method by the author because it provides reliability by using the parasitic capacitance of the MOS structure that helps in SEU tolerance. In two-input C-element, the voltage at the output port will be opposite to that of the input port voltage, whether it is at logic “1” or logic “0”, provided that the both the input voltages are same. Now, when two different input voltages are provided at the dual-input C-element, a high-impedance state is achieved at the output terminal and hence, the output remains unchanged. The leakage power consumption of the design is comparatively lower due to the presence of stacked NMOS transistors. In addition to this, since the design uses four pass transistors so that the bit line to the storage node transmission path can be reduced. As a result, the contention current reduces. The drawback of the design is that due to the presence of larger number of transistor count (eighteen transistors), it results in an overall larger area. The design also requires an improved layout design that will be able to improve the reliability of the circuit. Hence, an alternative approach is required.

6.3.20 | SIMR-18T design (Year: May 2023)
Na Bai et al., 2023 in [54] designed a stable radiation resistant (SIMR-18T) SRAM cell that consists of eighteen transistors (ten PMOSs and eight NMOSs) and four storage nodes of which two (P and PB) are redundant nodes that helps to store redundant information. The SIMR-18T design is an enhanced version of QUATRO-10T design in which two extra PMOS transistors (P5 and P6) at the core inverter, two additional PMOS transistors (P3 and P4) and NMOS transistors (N3 and N4) at the outer core branches and two addition PMOS access transistors (P1 and P2) are incorporated in the QUATRO-10T design. In the design, a new performance metric has been considered by the author that considers both the SEU recovery probability and DNU recovery probability while estimating the overall performance of the design. The drawback of this design is that due to the presence of more number of feedback loops, when the supply voltage falls below 1V, it results in more write delay. Due to the presence of stacked NMOS pull-down transistors and since the feedback loop is longer, the design takes more time to read the data and discharge in the bit-line. Hence, an alternative approach is required.

6.3.21 | RHWC12T design (Year: July 2023)
Rishabh Sharma et al., proposed an improved writing capability radiation tolerant (RHWC12T) design [58] that contains four storage nodes and consists of twelve transistors with four pull-up PMOS transistors, four pull-down NMOS transistors and four NMOS access transistors. Here, the author used two additional NMOS access transistors to improve the write operation, similar to WE-QUATRO and QUCCCE-12T design. In the design, when radiation strikes at the charge storage nodes such as Q and QB, the internal redundant nodes (S and SB) mostly remains unaffected and remains in their initial logic states. However, the drawback of this design is that it contains four sensitive nodes, thereby increasing the probability of SEU occurrence at those nodes and since every nodes are being surrounded by PMOSs and NMOSs, it results in larger number of node-pairs for DNU. Thus, the design has a higher probability of radiation strike not only at all its single nodes but also at multiple nodes, resulting in multiple node upsets. Hence, decreasing the probability of radiation particle strike at those sensitive nodes or node-pairs is essential, despite its recovery. So, we are looking for another design.

6.4 | FOURTH CATEGORY OF REVIEWED SRAM CELLS

6.4.1 | SERS design (Year: 2020)

Zhengda Dou et al., designed a 21 transistor radiation resistant (SERS) SRAM cell [64] containing six storage nodes. The design consists of six pull-up PMOS transistors, six pull-down transistors, three NMOS transistors in-between the inverter pairs and six NMOS access transistors. The design is capable of providing self-recovery from SNU and also provides self-recovery from all possible DNUS. The drawback of the design is that it contains higher number of sensitive nodes and node-pairs (six sensitive nodes for SNU and fifteen node-pairs for DNU), thereby increasing the chances of radiation strike probability. In addition to this, the design also consumes higher power, thereby, increasing the average power consumption and largest area occupancy due to larger number of transistor count. As a result, sensitive area along with the overall area also increases due to more transistor count.

6.4.2 | LPDNUR & HSDNUR design (Year: March 2023)

Shuo Cai et al., 2023 in [53] designed two radiation resistant SRAM cells named as LPDNUR and HSDNUR that consists of four storage nodes and uses a two-input C-element structure that helps not only to
provide recovery from the radiation effects but also, the technique is useful in reducing the average power consumption due to its stacking effect. Hence, both the designs consume lower leakage power in steady state. The LPDNUR design is a modified version of the previous CC18T design in which two additional NMOS transistors N3 and N5 have been added to the two-input C-element structure placed in-between. The design HSDNR has similar storage nodes as that of LPDNUR and uses one word line and the other one its complement for data transmission in single node by using NMOS and PMOS transistor combination with four additional transistors in parallel with NMOS that represents a transmission gate (TG). This approach has been able to increase the current driving capability and reduces the delay during the transmission of data. Thus, by using both NMOS and PMOS as single node data transmission, the access time reduces considerably. The drawback of this design is that it consists of more number of transistors (20 transistors for LPDNUR and 24 transistors for HSDNRUR), thereby increasing the overall area of the design. This approach can be useful in order to reduce the hold power dissipation along with reduction in access time along with providing recovery from SNU and DNU, but this design is not preferred for designing layout using lesser area.

6.4.3 | HRHS & HRHS_EV design (Year: June 2023)

Aibin Yan et al., 2023 in [56] designed two radiation tolerant cell HRHS18T and HRHS18T_EV consisting of eighteen transistors (six NMOSs, six PMOSs and six access transistors) having six storage nodes. In HRHS18T design, the author connected the gate of six NMOS pull-down transistors and six pull-up transistors to the storage nodes and the gate terminal of the six access transistors are attached to the word line. In the HRHS18T design, storage node I1 is connected to the gate of N2 and P6, I2 is connected to the gate of N3 and P5, I3 is attached to the N6 and P4 gate port, I4 is attached to the gate of N1 and P3, I5 is connected to the gate of N4 and P2 and I6 is connected to the gate of N5 and P1. As a result, the design possess good SEU recover capability. HRHS18T_EV is an enhanced version of the HRHS18T design. The HRHS18T_EV cell has been able to improve the write delay compared to HRHS18T design. In the HRHS18T_EV design, storage node I1 is connected to the gate of P2 and P6, I2 is connected to the gate of N1 and P3, I3 is connected to the N2 and N4 gate port, I4 is attached to the gate of N3 and N5, I5 is connected to the gate of P4 and N6 and I6 is connected to the gate of P1 and P5. Overall, both the design has been able to provide good results in terms of read delay and write delay. However, the drawback of this design is that due to the increase in the number of storage nodes, the probability of SEU occurrence increases along with an increase in the sensitive area and sensitive node-pairs (HRHS18T contains six-pairs in total and HRHS18T_EV contains fourteen node-pairs in total). Also with the increase in the number of transistors (eighteen transistor), the total area also increases and also results in high power consumption.

6.4.4 | SCCS-18T and SCCS-18T-EV design (Year: August 2023)

Aibin Yan et al., designed two sextuple cross-coupled SRAM radiation tolerant design [59] that contains six charge storage nodes and consists of eighteen transistors out of which six are pull-up PMOS transistors, six are pull-down NMOS transistors and the remaining six are NMOS access transistors connected across the storage nodes. The SCCS-18T design provides complete recovery from the radiation effect that can strike at a single node but provides partial DNU recovery. To address this issue, the author proposed a modified version of SCCS-18T design known as SCCS-18T-EV cell design that improves the DNU self-recoverability compared to the previous design. Thus, this new design can provide more recovery from its sensitive node-pairs. However, the drawback of these design is that it contains large number of sensitive nodes (six sensitive nodes), thereby increasing the chances of upset from radiation. Moreover, since all the nodes are surrounded by PMOSs and NMOSs, hence, it results in larger number of node – pairs for DNU (six sensitive node-pairs for SCCS-18T and eight sensitive node-pairs for SCCS-18T-EV), thereby, increasing the probability of upsets at multiple nodes as well. Additionally, due to large number of transistors present in the design, the area of the cell also increases along with increase in power consumption. Due to large number of sensitive nodes, the sensitive area also increases. Thus, there is a trade-off between the transistor count that increases the area and power consumption in order to provide better reliability and soft error robustness from the radiation effects. Hence, an alternative design is required that contains less number of sensitive nodes and sensitive
node-pairs and providing effective access time operations.
FIGURE 12. RHBD designs. (i) LPAR 8T [27]. (ii) Security-oriented 7T [7]. (iii) RHLR12T [57]. (iv) LPAR12T [9].

6.5 | FIFTH CATEGORY OF REVIEWED SRAM CELLS

6.5.1 | LPAR 8T design (Year: 2018)

Robert Giterman et al., proposed a symmetrical LPAR 8T SRAM cell [27] which is an improved version of the conventional 6T SRAM cell. In order to make the design side channel leakage power attack resilient and to produce similar standby current pattern for both ‘1’ storing and ‘0’ storing cases, the author added two additional transistors in which the gate terminals are grounded. As a result, the total leakage current
components becomes equal for both data storage states (‘0’ and ‘1’) and is resilient to LPA based SCA. However, the design possess the problem of lower noise margin due to an additional leakage current path from the supply voltage to ground.

### 6.5.2 Security-oriented 7T design (Year: 2019)

Robert Giterman et al., proposed a security oriented 7T SRAM cell [7] that uses a dual-phased write operation with the help of one extra PMOS transistor added to the conventional 6T design that reduces the correlation between write energies of write ‘1’ and write ‘0’, and a single power gate transistor has been used, thereby equalizing the charge between two storage nodes and providing PA resilient design. However, the correlation between written data and stored has decreased considerably.

### 6.5.3 RHLR 12T design (Year: 2023)

Debabrata Mondal et al., designed a radiation tolerant and LPA resilient RHLR12T design [57] that uses twelve transistors and four storage nodes to mitigate SEU as well as providing LPA resilience. The design is a modified version of the existing RHMD10T in which the author added two additional NMOS transistors in the RHMD10T design. The RHMD10T has mismatch in the leakage current components in ‘0’- storing state and ‘1’- storing state and hence, to equalize the total leakage current components, the RHLR12T design has been proposed that is LPA-resilient.

### 6.5.4 LPAR 12T design (Year: 2023)

Syed Farah Naz et al., designed new Schmitt trigger based LPAR 12T SRAM cell [9] which is a modified design of the existing ST-10T in which the author incorporated two additional access transistors N9 and N10 to the ST-10T design in order to equalize the number of subthreshold leakage current components to make it LPA resilient. The LPAR12T design aims to improve the problem of low noise margin that was existing in LPAR 8T SRAM cell and also improves the LPA resilience compared to ST-10T SRAM cell, since ST-10T was not resilient to LPA due to its unequal leakage current components. Hence, to overcome the stability issues and LPA based issue, LPAR 12T design has been proposed that possess equal leakage current components.

### 7 REVIEW OF DESIGNS PARAMETERS AND PERFORMANCE QUALITY METRIC COMPARISONS

In this section, based on the mentioned categories of RHBD SRAM cells in section 6, design metrics are being summarized as shown in Table 1. In order to measure the stable state and durability of the reported RHBD designs, design parameters such as Read Access Time, Write Access Time, and Static Noise Margin are shown. To test the tolerance and reliability of the RHBD designs, parameters such as Critical Charge (\(Q_{\text{crit}}\)) or soft error robustness along with the number of sensitive nodes for single node upset (SNU) recovery and multiple node upset (MNU) recovery has been presented in Table 1. Additionally, in order to gauge the reliability of the memory cell, factors such as leakage power dissipation has been presented. The overall performance of the designs and the combined effects of the parameters are dependent on performance quality metric as shown in equation (6).

#### 7.1 Read Access Time (RAT)

Read Access Time (\(T_{\text{RA}}\)) of SRAM cell is described as the interval of time at the WL rising edge when it reaches half of \(V_{\text{DD}}\) to the point where the difference in the voltage of bit lines becomes at least 10% of \(V_{\text{DD}}\) [33]. Read delay or read access time during read mode (\(T_{\text{RA}}\)) depends on the capacitance of bit lines and read current via the access transistors. The transistor sizing is defined by the cell-ratio (CR) and the value of CR must be higher to get a lower \(T_{\text{RA}}\).

#### 7.2 Write Access Time (WAT)

Write Access Time (\(T_{\text{WA}}\)) of SRAM is defined as the interval of time at the WL positive rising edge when WL reaches 50% of \(V_{\text{DD}}\) to the point at which the two charge storage internal nodes (Q as well as QB)
intersects [13]. In order to get a reliable write operation, the pull-up ratio (PUR) must be lower to get a higher $T_{WA}$ and higher write static noise margin (WSNM).

### 7.3 | Static Noise Margin (SNM)

The Static Noise Margin (SNM) helps to test the stability of SRAM cell. SNM is stated as the smallest amount of noise voltage capable of changing the value of a bit stored in an SRAM cell [13, 39, 60]. There are three types of SNM, i.e., Read Static Noise Margin (RSNM), Write Static Noise Margin (WSNM) and Hold Static Noise Margin (HSNM).

The possibility of a read failure can be measured by the RSNM of a memory cell. RSNM is a parameter used to assess the capacity of the memory cell to maintain its stable state during read operations. In order to get the RSNM curve, a noise voltage in DC mode is provided at one of its charge storage nodes (Q or QB), keeping both the bit lines already pre charged to $V_{DD}$ and then the VTC curve is observed. The RSNM of an SRAM cell mainly depends on the CR value and read path.

Write Stability of all the cells are measured by the WSNM of a memory cell. To get the WSNM curve, a noise voltage in DC mode is inserted at one of the input of the inverter-pair and simultaneously the respective storage node VTC curve is observed, and same goes to another input pair of the inverter.

The data holding capability in standby condition of all the cells are measured by the HSNM of SRAM cell. Similar to RSNM and WSNM, noise voltage as type DC is provided at one of the internal storing nodes.

### 7.4 | Standby Leakage Power Dissipation

The overall power dissipated in a memory design greatly depends on the leakage power since majority of the cache memory remains in standby condition. The standby leakage power dissipation can be measured under the hold condition of the memory cell [40], in other words, the WL is transitioned to logic ‘0’, and both the bit-lines are initially charged to the supply voltage. The power calculated across this BL and BLB is termed as the leakage power dissipation.

**TABLE 1: Overall Summary of all RHBD SRAM designs**

| SI No. | Memory cell | Year | Technology Nodes | $V_{DD}$ (V) | Access Times (ps) | Access Times (ps) | Static Noise Margins (mV) | Static Noise Margins (mV) | Leakage Power (nW) | Area (um$^2$) | $Q_{crit}$ (fC) | Sensitive Nodes for SEU Recovery | Sensitive Node-pair for MNU |
|--------|-------------|------|------------------|--------------|-------------------|-------------------|--------------------------|--------------------------|------------------|---------------|-----------------------------|---------------------------------|
| 1      | QUATRO2009 10T [30] | 2009 | 90nm             | 0.9          | RAT 109.40        | WAT 26.07         | RSNM 81                  | WSNM 195.3             | 4.86             | 4             | 6                          | 4                                |
| 2      | PS-10T, NS-10T [31] | 2012 | 180nm            | 1.8          | 100.1, 125.9      | 21.29, 20.91      | 135, 70                  | 240.6, 242.7           | 4.3, 3.5         | 4, 4            | 6, 6                        | 4                                |
| 3      | RHM-12T [13] | 2014 | 65nm             | 1.2          | 66.20             | 5.50              | 8.7                      | 621.7                   | 23.49            | 3             | 3                          | 3                                |

45
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<th>Access Times (ps)</th>
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TABLE 2: Overall Radiation Tolerance, Resilience and LPA Summary of all RHBD SRAM designs
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7.5 | Layout Area ($A_{\text{total}}$) and SEU Probability Occurrence ($P_s$)

In order to compare the area and get a detailed analysis, layout is being designed. In the process of eliminating the possibility of upsets at multiple node at a single radiation strike, the node pairs in the layout should maintain a minimum spacing of 0.6um, 1.62um and 2um between NMOS-PMOS, PMOS-PMOS and NMOS-NMOS, in order to avoid charge sharing [61]. The minimum distance between these transistors is targeted at the drain region of the OFF transistors at the sensitive nodes that changes value or state due to radiation. Hence, in layout, if minimum distance is maintained during layout, then the chances of multiple node upsets from a single strike get reduced considerably. The RC parasitic extraction is done from the layout.

The probability of occurrence of an SEU [13] is defined as:

$$P_s = \frac{A_{\text{sensitive}}}{A_{\text{total}}}$$(4)
where, \( A_{\text{sensitive}} \) is the sensitive area of the design and \( A_{\text{total}} \) is the overall area of the design. In order to avoid SEU as much as possible, the \( P_S \) of the memory cell needs to be as low as possible. Hence, lower the probability occurrence value, lesser will be the probable chances of a node being impacted by a single event upset. Lesser number of sensitive nodes leads to lower \( P_S \) and large area overhead also leads to less \( P_S \). The sensitive area (\( A_S \)) also decreases with decrease in the number of nodes which are sensitive.

### 7.6 | Critical Charge (\( Q_{\text{crit}} \))

To perform the simulation for the impact of radiation on semiconductor devices, double exponential current source is being employed [13, 40]. This double exponential current pulse is being applied across the node of a circuit which are sensitive to validate the robustness and tolerance of the SRAM cell’s soft error as stated in equation (1). Critical charge (\( Q_{\text{crit}} \)) is stated as the lowest amount of charge accumulated at a sensitive node that can flip the original content stored in the memory cell. At the time of evaluation, the \( Q_{\text{crit}} \) that contains the lowest value among all the nodes which are sensitive gives the effective \( Q_{\text{crit}} \) of the cell. The equation for calculating the critical charge is given as:

\[
Q_{\text{crit}} = \int_0^{T_{\text{crit}}} I_{\text{inj}}(t) \, dt \tag{5}
\]

where \( I_{\text{inj}}(t) \) is the exponential current pulse injected at sensitive node for the recovery analysis at a single event, \( T_{\text{crit}} \) is the critical time at which the voltage across \( Q \) and \( QB \) becomes equal as can be seen in Fig. 13(b). The non-flipping state takes place before the state of the storage node gets flipped as shown in Fig. 13(a). The minimum magnitude and duration of injected current pulse that is enough to flip the logic state of the storage node is being taken into account. Thus, \( Q_{\text{crit}} \) is determined by doing the integration of the current magnitude between the time intervals 0 to \( T_{\text{crit}} \). Hence the condition for evaluating \( T_{\text{crit}} \) should satisfy \( V_Q = V_{QB} \).
FIGURE 13. (a) Non-flipping state representation of conventional 6T SRAM cell (b) Graphical representation defining critical charge for conventional 6T SRAM cell.

7.7 | SEU and MNU Tolerance and Resilience

The radiation-hardened SRAM cells are further categorized into four types: SEU Tolerant, SEU Resilience, MNU Tolerant and MNU Resilience as shown in Table. 2. As mentioned in Section. 3, the radiation in an SRAM cell can cause SEU and MNU. MNU occurs when two or more sensitive node-pair present in the cell gets affected. The number of sensitive nodes for SEU and sensitive node-pair for MNU are shown in Table. 1. The latch of an SRAM cell is called SEU Tolerant when one of the internal nodes that gets flipped by a radiation particles does not change the output of the latch. The flipped node can be called SEU Resilience when one of the sensitive nodes that gets flipped does not change the output of the latch. Similarly, when two or more sensitive nodes that gets flipped does not affect the output of the latch, it is tolerant to MNU and if pair sensitive nodes are flipped, and the latch output will not be affected, then the flipped nodes can be resilient and is called MNU Resilience [60].

7.8 | LPA Resilient
The major cause of side channel attack (SCA) is the difference in leakage current distribution in the memory cell [9]. This leakage current flow is the function of logic-“0” and logic-“1” stored in the memory cell. If the number of transistors through which subthreshold leakage current flows is equal, then the cell is resilient to LPA, otherwise, there are high chances of LPA-based SCA and is not resilient to LPA as shown in Table. 2. Fig. 13(a) and 13(b) shows the unequal leakage current component distribution for RHMD10T and equal leakage current component distribution for RHLR 12T SRAM cell in hold mode. Hence, RHLR 12T is LPA resilient.

Figure 14. (a) Schematic of RHMD10T SRAM cell during hold mode with main leakage current components (b) Schematic of RHLR 12T SRAM cell during hold mode with main leakage current components.

7.9 | Performance Quality Metric (PQM)

In today’s technology, a cell that contains ideal area, enhanced SNM, soft-error tolerance, ideal power dissipation and optimum delay is preferred. Considering all these parameters, to access the complete performance of the cell, and to access the quality of the overall cell in terms of both stability and reliability, a new metric of design called performance quality metric (PQM) comes into play as shown in equation (6).

\[
PQM = \frac{Q_{\text{crit}} \times RSNM \times WSNM \times HSNM}{P_{\text{Leakage}} \times P_{\text{Dynamic}} \times T_{WA} \times T_{RA} \times \text{Area}}
\]

(6)

8 | CONCLUSION

This paper delves into the exploration of radiation-hardened and attack resilient memory circuits, spanning the last two decades. A noteworthy observation is that most research articles do not achieve complete immunity to single event multiple node upsets (SEMNU) as well as side channel attack (SCA). Additionally, we consolidate various designs, outlining their fundamental parameters and offering metrics to assess the stability, reliability and security of memory cells. Ultimately, our findings underscore a trade-off between
performance, resilience to SEU/SEMNU parameters and leakage power attack resilient behaviour. Consequently, bridging this gap becomes imperative for advancing this research domain.

References:


36. J. Jiang, Y. Xu, W. Zhu, J. Xiao and S. Zou, "Quadruple Cross-Coupled Latch-Based 10T and


50. R. Shekhar, C. I. Kumar, “Design of highly reliable radiation hardened 10T SRAM cell for low voltage applications,” Integration, Volume 87, 2022, Pages 176-181, ISSN 0167-9260, doi.org/10.1016/j.vlsi.2022.07.004

