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Abstract

This article presents a novel scheme for condition monitoring of dc-link capacitors in modular multilevel converters (MMCs). The proposed solution uses estimated capacitance values of the dc-link capacitors for indicating their state-of-health (SoH). Moreover, a comparative approach is proposed where the estimated capacitance of all submodule capacitors are used to separate parameter drifts caused by aging from parameter drifts caused by other factors such as temperature change. It is shown in simulation and experimental results that a short-term equal drift in all capacitance estimates can be a result of factors other than aging. However, a drift in the capacitance of one capacitor compared to the average capacitance of all submodules may be attributed to aging of that specific unit. Using the proposed comparative technique, there is no need for additional temperature sensors to incorporate the effect of temperature variations on the online estimations. Simulation and experimental results prove an overall estimation error of less than 1\% when applying the proposed comparative technique.
Practical Online Condition Monitoring of DC-Link Capacitors in Modular Multilevel Converters: A Comparative Approach

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Abstract—This article presents a novel scheme for condition monitoring of dc-link capacitors in modular multilevel converters (MMCs). The proposed solution uses estimated capacitance values of the dc-link capacitors for indicating their state-of-health (SoH). Moreover, a comparative approach is proposed where the estimated capacitance of all submodule capacitors are used to separate parameter drifts caused by aging from parameter drifts caused by other factors such as temperature change. It is shown in simulation and experimental results that a short-term equal drift in all capacitance estimates can be a result of factors other than aging. However, a drift in the capacitance of one capacitor compared to the average capacitance of all submodules may be attributed to aging of that specific unit. Using the proposed comparative technique, there is no need for additional temperature sensors to incorporate the effect of temperature variations on the online estimations. Simulation and experimental results prove an overall estimation error of less than 1% when applying the proposed comparative technique.

Index Terms—Dc capacitor, health estimation, modular multilevel converter, online monitoring, reliability

I. INTRODUCTION

MODULAR multilevel converters (MMCs) are regarded as the most suitable solution for high-voltage and high-power applications [1], [2]. The modular design of MMCs enable the generation of voltages and currents with low total harmonic distortions (THDs). In grid-connected applications, the large number of MMC submodules justifies low switching frequencies of semiconductors compared to the two-level and three-level converter solutions [3]. For a reasonably high number of submodules, the possibility of using switching frequencies close to the fundamental frequency of the network has been reported [4]. Opting such low switching frequencies significantly improves the efficiency of MMCs. One of the disadvantages of MMC converters is that each submodule capacitor must be designed to withstand large voltage ripples, especially of the fundamental and second-order frequencies [5]. This buffering of high energies can only be accomplished by large capacitor modules. This makes the submodule capacitors one of the more expensive components in MMCs [6]. Considering that MMCs are typically used in applications where high reliability and high availability is required [7], it is important to monitor and protect sensitive components that are essential to their operation. The most critical components in an MMC submodule that are subject to high power currents leading to electro-thermal degradation are the semiconductors and the submodule capacitors [8]. Although MMCs are typically designed to have a fault-ride-through operation after the failure of one or more submodules by introducing redundancies [9], it is beneficial to have accurate online monitoring of the state-of-health (SoH) of its critical components. This SoH data may then be used for predictive maintenance, selectively reducing component stress, or controlled bypassing of degraded components. Consequently, realizing accurate condition monitoring (CM) techniques results in increased reliability and availability, and reduces costs related to unscheduled maintenance.

Condition monitoring of semiconductor devices in MMCs has been addressed in the literature [10]. It has also been shown that utilizing the submodule redundancies, highly accurate parameter estimations can be achieved for CM of semiconductor devices [11]. Monitoring submodule capacitors is equally important as they are one of the main power components in MMCs. Several publications have addressed this importance, and proposed various techniques for their online CM [12]–[16]. The capacitors used for high-power MMCs are typically of the metalized polypropylene film (MPPF) type [17]. In these capacitors, a capacitance reduction of 5% is shown to be the end-of-life (EoL) criteria [18]. In lower power applications, aluminum electrolytic (AE) capacitors and multi-layer ceramic (MLC) capacitors have been used for dc-links. For AE capacitors, the EoL is defined as 20% reduction in capacitance and/ or 200% increase in ESR, while for the MLC capacitors, a 10% reduction in capacitance is reported as EoL [18]. Although degraded MPPF capacitors have also been shown to have an increase in their ESR [19], [20], this value is very small in high-current applications [21], and difficult to track accurately through online measurements. Nevertheless, the online estimation of capacitance must be sufficiently accurate in order to precisely detect the 5% drift in capacitance.

In recent, CM of dc-link capacitors in MMCs has received considerable attention. In [22], online tracking of the ESR has been experimentally shown. However, the level of ESRs in that study are orders of magnitude larger than what high-power capacitors typically have have [21]. A method based on detecting the time constant of resistive-capacitive (RC) discharge is presented in [23] where a modified operation of each submodule is necessary to assure accurate estimations, and a known resistive element must be introduced to realize the CM techniques. Similarly, in [24], a known resistive element...
must be introduced to the circuit in order to realize the CM method.

The use of reference submodules has been proposed in [25] where a submodule with a known capacitance is given the same switching pattern as another submodule in the same arm.

The solutions provided in the literature are typically application specific, where a specific switching frequency (typically high switching frequencies of over 5 kHz) and low measurement noise are considered. The frequency-based method presented in [26] is one of the first papers to thoroughly address the issue of estimation accuracy in the presence of high measurement noise. In that study, selected frequency content of the voltage and estimated current of the submodule capacitor is used to provide accurate estimations. Moreover, the signal-to-noise ratio of the measurements are increased by integrating their phasor values over time. The solution works well for a wide range of switching frequencies, and under different load conditions. In [17], a thorough comparison is made between the frequency based estimation of [26] and the RLS-based estimation method. Although both methods have been shown to be highly accurate in the presence of measurement noise and when subject to various loads, the estimation error of the RLS method is shown to increase when high switching frequencies are used. Nevertheless, for MMCs used in FACTS and high-voltage dc (HVDC) applications both the RLS method of [17] and the frequency-based estimation method of [26] are shown to be accurate and robust, and do not suffer from the aforementioned disadvantages of other proposed methods.

Regardless of how accurately the capacitance of each submodule is estimated, there is one major element that has been widely neglected in the literature which can distort the estimations. That is the effect of temperature. The capacitance of MPPF capacitors are reported to have a negative temperature coefficient [21], while the capacitance of AE capacitors typically have a positive temperature coefficient [27]. Consequently, changes in the ambient temperature, as well as changes in the converter load may result in temperature variation of the capacitors. This in turn causes variations in the measured capacitance. If not compensated for, such variations may be wrongly attributed to degradation of the monitored capacitor. In [21], a dynamic margin is proposed to compensate for temperature variations, however, this method might cause overcompensation if the thermal model of the capacitor is not correctly modelled. In this paper, a novel SoH estimation approach is proposed that enables online compensation for temperature-related variations of the estimated capacitance values. The proposed method utilizes the SoH information of all submodule capacitors in one arm to correctly assess the health state of each capacitor. This comparative approach has a few unique advantages which distinguishes it from the state of the art solutions:

- A major advantage of the proposed solution is that no temperature sensors are required for its operation. This is especially valuable for large capacitor banks without any suitable or accessible point to accurately monitor their internal temperature.
- Pre-characterization of the submodule capacitors is not needed. Also, there is no need to have an accurate thermal model of the capacitor modules. The comparative approach provides sufficient data for accurate online estimation of the SoH, even under variable temperatures of the capacitors.
- Since the capacitance estimation is conducted using the methods described in [17], [26], the estimated values enjoy similar accuracies, with errors lower than 1% over a wide range of switching frequencies and converter operations. It is also suitable for a wide range of MMCs used for FACTS and HVDC applications.
- The solution allows uninterrupted operation of the converter for the purpose of measurements and estimations.

The proposed solution in this paper is mainly demonstrated on converters with MPPF or AE capacitors; however, the type of capacitor is irrelevant to the proposed methods. For CM purposes, any capacitor that has a temperature-dependent capacitance requires online compensation of effects caused by varying temperatures. The proposed solution can effectively identify the capacitance of any capacitor unit, and minimize the temperature-related variations of its capacitance in MMCs.

This paper is organized as follows: Section II presents the converter topology and the control system used for studying the online capacitor estimation technique. The selected estimation method is explained in Section III. The proposed comparative concept is presented in Section IV, where its efficacy is proven analytically and by simulation. The experimental setup and experimental verifications are summarized in Section V, and the conclusions are reported in Section VI.

II. Converter System

The proposed capacitor monitoring algorithm is mainly developed for MMC-based STATCOMs. These STATCOMs are the preferred solution in the industry due their high-efficiency and high power-quality [28]. The Y-STATCOM [29], D-STATCOM [30], and the double-Y-STATCOM [31] are the most popular MMC-based STATCOM topologies. For simplicity, the proposed solutions of this paper are verified on a single-phase MMC-based (SPMMC) STATCOM; however, these solutions can be separately used for each arm of multi-phase MMC-based STATCOMs. The circuit diagram of the SPMMC is shown in Fig. 1. This converter consists of one arm of series-connected full-bridge submodules. The full-bridge submodule shown in Fig. 1 comprises four semiconductor switches, namely \(sw_i, i = \{1, 2, 3, 4\}\). A switching function \(s_i, i = \{1, 2, 3, 4\}\) is attributed to each \(sw_i\) device, where \(s_i = 1\) and \(s_i = 0\) correspond to the ON-state and OFF-state of the switch \(sw_i\), respectively. Depending on the state of the semiconductor devices, the submodule can be inserted in the positive direction \((v_{out} = +v_c)\), in the negative direction \((v_{out} = -v_c)\), or bypassed \((v_{out} = 0)\). In this study, only full-bridge submodules are considered. However, similar algorithms can be applied to MMCs with half-bridge submodules as well.

The overall control system of the SPMMC used in this paper is shown in Fig. 2. The control system features a
phase-lock-loop (PLL), a proportional-resonant (PR) current controller, and a capacitor voltage controller. The capacitor voltage controller is divided into two parts: the sum capacitor voltage/energy control and the voltage balancing control. For the sum energy controller, the sum of all submodule capacitor voltages $v_{\Sigma}^{c}$ are initially filtered using a low-pass filter (LPF) and a band-stop filter (BSF). The filtered value is then compared to a reference value $v_{\Sigma}^{\ast}$. The difference is passed through a proportional-integral (PI) controller before creating the direct-current reference $i_{d,\Sigma}^{\ast}$. This reference is common for all submodules. The voltage difference between the submodules is compensated by comparing the filtered capacitor voltage of every submodule $v_{c,i}$ to the average voltage of all submodule capacitor voltages $v_{c}$. The difference is passed through a PI controller, and becomes the individual direct-current reference component $i_{d,\Delta}^{\ast}$. This element may be different for every submodule, and becomes zero when all submodules have the same average voltage. The reactive power reference is directly generated using a reference $I_{q}^{\ast}$ for the quadratic-current signal $i_{q}^{\ast}$.

The SPMMC is operated in current-control mode [32], [33]. The controller used in this study is a proportional-resonant controller. The closed-loop current controller features a single current sensor that is series-connected with the chain-link of submodules. A PR controller with a proportional gain $K_{p}$ and a resonant gain $K_{r}$ are used for governing the current. The resonance frequency of this controller is set to the grid angular frequency $\omega_{0}$. At each time step of the control system, the sum of the reference currents $i_{q}^{\ast}, i_{d,\Delta}^{\ast}$ and $i_{d,\Sigma}^{\ast}$ are compared with the arm current $i_{arm}$ and passed through the PR controller to generate the voltage reference of the submodules. The grid voltage $v_{g}$ is measured and used as a feed-forward to enhance the dynamics of the control system. The reference signals of all submodules are divided by the sum capacitor voltages before being modulated in order to compensate for the capacitor voltage ripples [32]. Due to its ease of analysis, a phase-shifted carrier-based pulse-width modulation (PSC-PWM) technique is opted for this study. The system parameters used for simulating the SPMMC are presented in Table I.

III. CAPACITOR MONITORING SCHEME

In MMCs, the capacitance value of dc-link capacitors are a more suitable parameter for their online health estimation due to the inherently small ESRs of these capacitors [17]. In [17], two suitable methods of dc-link capacitance estimation for MMCs are presented and compared. Both methods, namely the RLS estimation method, and the frequency-based estimation technique are shown to provide capacitance estimations with less than 1% error. Moreover, both methods have been shown to have high estimation accuracies under variable load conditions, and under different switching frequencies of the converter. In this study, the frequency-based estimation algorithm is used. In this method, specific frequency content of the measured capacitor voltage and estimated capacitor current are extracted, and utilized for estimating the capacitance at that specific frequency. In the first step, the specific frequency content of the capacitor voltage $v_{c}$ and current $i_{c}$ is mirrored onto a direct-quadratic ($dq$) reference frame. For a selected angular frequency $\omega_{p}$, this mirroring is achieved through

![Figure 1. Single-phase MMC-based STATCOM topology and its full-bridge submodule.](image)

![Figure 2. Control system used for governing the operation of the SPMMC in Fig.1.](image)

<table>
<thead>
<tr>
<th>Table I</th>
<th>SYSTEM PARAMETERS USED FOR STUDYING THE SPMMC STATCOM TOPOLOGY</th>
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<tbody>
<tr>
<td>Nominal power</td>
<td>Symbol</td>
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<tr>
<td>Nominal voltage</td>
<td>$V_{g}$</td>
</tr>
<tr>
<td>Cell capacitance</td>
<td>$C_{cell}$</td>
</tr>
<tr>
<td>Capacitor ESR</td>
<td>$ESR$</td>
</tr>
<tr>
<td>Number of cells</td>
<td>$N$</td>
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<tr>
<td>Arm inductance</td>
<td>$L_{arm}$</td>
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<td>Carrier frequency</td>
<td>$f_{c}$</td>
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multiplying $v_c$ and $i_c$ by $\sin(\omega_p t)$ and $\cos(\omega_p t)$, as follows,

\begin{align*}
v_{c,a} &= v_c \cos(\omega_p t) \\
v_{c,b} &= v_c \sin(\omega_p t) \\
i_{c,a} &= i_c \cos(\omega_p t) \\
i_{c,b} &= i_c \sin(\omega_p t).
\end{align*}

(1)

Any harmonic content of the angular frequency $\omega_p$ in $v_c$ is transformed to direct components in $v_{c,a}$ and $v_{c,b}$; whereas all other harmonic content of $v_c$ appear as non-direct or oscillatory terms. The same can be said for $i_{c,a}$ and $i_{c,b}$. In SPMMCs, the dc-link capacitor is known to have a dominant second order harmonic component, $2\omega_0$ [17]. Hence, this frequency is chosen for the capacitance estimation.

In order to increase the signal-to-noise ratio (SNR) of the harmonic components at $2\omega_0$, the signals of (1) are integrated over time. It is shown that integration periods that are integer multiples of the fundamental frequency lead to the largest harmonic components at $2\omega_0$; whereas any harmonic content of the angular frequency $\omega_p$ with $2\omega_0$ in (1) and integrating the equations over $N_p$ periods of the fundamental frequency leads to

\begin{align*}
V_{c,a} &= \int_0^{N_p T_0} v_c \cos(2\omega_0 t) dt \\
V_{c,b} &= \int_0^{N_p T_0} v_c \sin(2\omega_0 t) dt \\
I_{c,a} &= \int_0^{N_p T_0} i_c \cos(2\omega_0 t) dt \\
I_{c,b} &= \int_0^{N_p T_0} i_c \sin(2\omega_0 t) dt,
\end{align*}

(2)

where $T_0$ represents the time period of the fundamental frequency component. The parameters $V_{c,a}$, $V_{c,b}$, $I_{c,a}$, and $I_{c,b}$ in (2) are an approximation of the Fourier Transform (FT) of the functions $v_c$ and $i_c$, at the angular frequency $2\omega_0$; the difference being that in FT, the integration is conducted over $\pm\infty$.

Finally, the capacitance value of each dc-link capacitor can be accurately estimated using the amplitudes of the integrated $dq$ components of $v_c$ and $i_c$ as follows

\[ C = \frac{\sqrt{I_{c,a}^2 + I_{c,b}^2}}{2\omega_0 \sqrt{V_{c,a}^2 + V_{c,b}^2}}. \]

(3)

Larger time windows of integration result in higher SNR values of (2), and in turn, higher estimation accuracies in (3) [17].

IV. EFFECT OF TEMPERATURE VARIATIONS AND THE COMPARATIVE APPROACH

The capacitance of MPPF capacitors has a negative temperature coefficient [21]. This means that at higher temperatures, the capacitance value drops. If this effect is not compensated for, the health estimation algorithm might incorrectly attribute the capacitance variation to component degradation. Hence, the effect of temperature variations are not negligible in health estimation of capacitors, and lead to erroneous predictions of the state of health (SoH). The use of dynamic margins for temperature compensation shown in [21] can reduce the estimation errors, but will not fully compensate them. It is also possible to use temperature sensors and lookup tables to compensate for the temperature variations; however, this requires additional sensors. Moreover, measuring the internal temperature of capacitors in online operation is not trivial. Hence, ideally an estimation method is needed that can separate the capacitance drift caused by temperature variations from that caused by degradation without the use of additional sensors. The comparative approach presented in this paper provides these functionalities.

A. The Comparative Approach

All series connected submodules of an MMC are designed to be as similar to each other as possible. This provides design modularity, where all submodules are expected to operate similarly when subject to the same voltages and currents. It is also desirable that series connected submodules experience an equal voltage and power stress. Equal distribution of voltage and power stress does not always naturally occur in MMCs and must be imposed with suitable control algorithms. If the dc-link capacitors in all submodules are controlled to experience the same voltage and power stress over time, it is expected that they also experience similar thermal stress. Under this condition, the capacitors of all submodules are expected to have similar thermal dynamics. Consequently, variations that occur in CM parameters of all dc-link capacitors for short periods of time can be attributed to some phenomena other than individual capacitor degradation. This concept is used in this paper were estimated capacitance values of all dc-link capacitors in one arm are continuously compared to each other. For a correctly designed converter system, all submodule capacitors should not significantly degrade simultaneously. Any short-term deviation from the initial capacitance value that occurs in all submodule capacitors can then be attributed to non-aging phenomena. Although unlikely, capacitance variations in all submodule capacitors that are sustained over long periods of time may still be attributed to health degradation. What is regarded as short-term and long-term is dependent on the thermal time constant of capacitors and expected ambient temperature variations; therefore, this window of time is application-specific. On the other hand, if the capacitance of one submodule deviates from the average of all capacitance values in the same arm, this deviation may be attributed to degradation of that specific capacitor. This hypothesis is true only if the submodule capacitors of one arm are controlled to experience the same internal losses, as well as the same ambient temperature. Whether the MMC station is established indoors or outdoors, it is reasonable to expect that the ambient temperature is the same for all submodule capacitors. Hence, what remains is to assure that the internal thermal stress of all submodule capacitors in one arm are equal. In this paper, a PSC-PWM modulations is used. This modulation is known to facilitate equal voltage sharing among submodules of one chain-link. The main requirement for this is to have a carrier frequency that is a non-integer multiple of the fundamental frequency [34]. In this paper, we show that this is also a
sufficient requirement for equal distribution of average losses among submodule capacitors of the same converter arm.

B. Proof of Concept

Considering a reference voltage of $M \cos(\omega_c t)$, the switching signals of $s_3$ and $s_4$ modulated with the PSC-PWM can be described as,

$$s_3 = \frac{1}{2} + \frac{1}{2} M \cos(\omega_c t - \pi) +$$
$$\frac{2}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_n(m \frac{\pi}{2} M) \sin([m + n] \frac{\pi}{2}) \times$$
$$\cos[m(\omega_c t + \theta_c) + n\omega_0 t - \pi],$$

and,

$$s_4 = \frac{1}{2} + \frac{1}{2} M \cos \omega_0 t +$$
$$\frac{2}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_n(m \frac{\pi}{2} M) \sin([m + n] \frac{\pi}{2}) \times$$
$$\cos[m(\omega_c t + \theta_c) + n\omega_0 t],$$

where $J_n(x)$ is the Bessel function of order $n$ and argument $x$, and $M$ is the modulation index [35]. In a chain link of submodules, the only difference between the switching signals of similarly positioned switches is the angle of the modulating carrier signal, $\theta_c$. For an arm with $N$ submodules, optimum harmonic cancellation is achieved when $\theta_c$ of every two adjacent submodules are set to be $180^\circ/N$ apart [35]. Under this condition, the only harmonics remaining across the cascaded submodules are the sideband harmonic components centered around the $2N^{th}$ carrier multiples. Assuming that each submodule is charged with a direct voltage $V_c$, the total instantaneous arm voltage can then be represented as,

$$v_{arm} = [N MV_c \cos \omega_0 t +$$
$$\frac{4V_c}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} J_{2n-1}(m\pi M) \cos([m + n] \pi) \times$$
$$\cos[2Nm\omega_0 t + (2n - 1)\omega_0 t]].$$

Consequently, a low total harmonic distortion (THD) is achieved for the output voltage of the converter.

The arm current of an MMC is typically controlled in closed-loop to follow a desired fundamental reference, and also to minimize low-order harmonics. Considering that each arm of an MMC is also equipped with a large inductor, the current THD in MMCs is very low, such that the high-frequency content of the arm current are negligible compared to the fundamental component [36], [37]. It is therefore reasonable to represent the arm current as a pure sinusoidal waveform. This assumption helps in simplifying the equations. Hence, the arm current is hereafter described as

$$i_{arm} = \hat{i} \cos(\omega_0 t + \phi),$$

where $\phi \approx \pm 90^\circ$ in MMC-based STATCOMs.

The instantaneous current passing thorough the dc-link capacitor of each submodule can be estimated using the measured arm current and the switching state of the four semiconductor modules. In Fig. 1, the current $i_c$ can therefore be represented as,

$$i_c = i_{arm}(s_1 s_4 - s_2 s_3).$$

(7)

Omitting the negligible effect of switching dead-time, (7) can be represented as,

$$i_c = i_{arm}[(1 - s_3) s_4 - (1 - s_4) s_3]$$
$$= i_{arm}(s_4 - s_3).$$

(8)

Substituting $s_4$ and $s_3$ in (8) with (4) results in,

$$i_c = i_{arm}[M \cos \omega_0 t +$$
$$\frac{4}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} J_{2n-1}(m\pi M) \cos([m + n - 1]\pi) \times$$
$$\cos[2m(\omega_c t + \theta_c) + (2n - 1)\omega_0 t]].$$

For simplicity, (9) is henceforth described as,

$$i_c = i_{arm}[k_1 \cos \omega_0 t +$$
$$\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} k_2(m, n) \cos[2m(\omega_c t + \theta_c) + (2n - 1)\omega_0 t]],$$

(10)

where, $k_1 = M$, and $k_2(m, n) = 2/m\pi J_{2n-1}(m\pi M) \cos([m + n - 1]\pi)$.

Substituting $i_{arm}$ from (10) with (6) yields

$$i_c = \frac{k_1}{2} \left[ \cos \phi + \frac{k_2}{2} \cos(2\omega_0 t + \phi) \right] +$$

$$\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{k_2(m, n)^2}{2} \cos[2m(\omega_c t + \theta_c) + 2n\omega_0 t + \phi] +$$

$$\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{k_2(m, n)^2}{2} \cos[2m(\omega_c t + \theta_c) + (2n - 2)\omega_0 t - \phi].$$

(11)

1) Conduction losses: Capacitor losses are typically modelled by their equivalent series resistance (ESR) value, $r_c$. The ESR consists of both dielectric losses and stray resistance of the conductive material [21]. For a known $r_c$, the instantaneous conduction losses of dc-link capacitors can be calculated as

$$p_c = r_c i_c^2.$$

(12)

It is evident from (11) and (12) that the only difference in the instantaneous power loss of different submodule capacitors is governed by the elements containing the term $\theta_c$.

Dc-link capacitors used in MMCs are bulky, resulting in high thermal capacitance. This results in slow temperature changes as a result of internal losses. Hence, in order to assess the effect of conduction losses on temperature changes in dc-link capacitors, the average power loss is a more suitable parameter than instantaneous losses. Average power losses,
represented by the parameter $p_c$, are defined as direct (non-oscillatory) elements of $\rho_c$. Substituting $i_c$ in (6) with (11) results in

$$p_c = (I_1 + I_2 + I_3 + I_4)^2 r_c. \quad (13)$$

Equation (13) contains self-multiplication terms such as $I_1^2$, and cross-multiplications such as $I_2 I_3$. There are also self-multiplication and cross-multiplication of all the terms in $I_2^2$ and $I_3^2$. Under the condition that $\omega_c$ is a non-integer multiple of $\omega_0$, none of the cross-multiplications would contain a direct component; hence, they do not appear in the average value of the capacitor losses. Thus, (13) becomes

$$p_c = \left(\frac{k_1^2 \cos \phi}{2}\right) + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2} \left(\frac{k_2(m,n) i_c}{2}\right)^2 + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2} \left(\frac{k_2(m,n) i_c}{2}\right)^2 r_c. \quad (14)$$

Under the condition of $\omega_c \neq k \omega_0, k \in \mathbb{Z}$, there are no terms containing the parameter $\theta_c$ in the average power loss of any submodule capacitor described in (14). Consequently, assuming that all dc-link capacitors have the same ESR value, under the condition of $\omega_c \neq k \omega_0, k \in \mathbb{Z}$, all submodule capacitors of one MMC arm are subject to the same average power losses.

2) Eliminating Temperature Effects: The SPMMC of Fig. 1 is developed in MATLAB/Simulink using the parameters of Table I. A simplified thermal model shown in Fig. 3 is considered for each capacitor. Due to the large time constant of these thermal models, much smaller thermal capacitance is considered for the simulations [21]. Specifically, the metalized layer is chosen to have a thermal capacitance of $c_{th,1} = 15 \text{J/C}$, and the other components in the capacitor tank are given an overall thermal capacity of $c_{th,2} = 60 \text{J/C}$. This results in the internal capacitor temperature reaching a steady-state value much faster, but does not interfere with the main concepts of this paper. The temperature coefficient of the selected MPPF capacitor is extracted from the datasheet of the manufacturer and depicted in Fig. 4 [21]. Similarly, the thermal resistors are based on the manufacturers data and chosen to be $r_{th,1} = 0.04^\circ\text{C/W}$, and $r_{th,2} = 0.04^\circ\text{C/W}$.

For the same ESR value, the estimated capacitance of all submodules are estimated using (2) and (3) over $N_p = 100$ fundamental periods. Hence, after every 100 fundamental periods of time, a new capacitance estimation is available for all submodule capacitors. The converter’s power reference is temporarily changed from 0.2 p.u. to 1 p.u. and then returned back to 0.2 p.u. During this time, the internal temperature of all capacitors increases because of the increased conduction losses. This change of temperature causes a reduction of capacitance according to Fig. 4. The internal temperature change as well as the estimated capacitance value of all $N$ submodule capacitors are shown in Fig. 5. Moreover, the variation of each estimated capacitance is depicted in Fig. 6(a). In this figure, each estimated capacitance is per-unitized using their initial capacitance as the base value. In Fig. 6(b) each estimated capacitance is compared to the average capacitance of all dc-link capacitors of one arm using

$$c_{comp,i} = \frac{c_i}{\sum_{j=1}^{N} c_j / N}. \quad (15)$$

Two important conclusions can be made from Fig. 6:

1) Under the aforementioned conditions, all submodule capacitors are subject to the same average temperature change.

2) The changes in the capacitance value as a result of temperature variations can be accurately identified using the comparative approach: comparing each estimated value to all estimated capacitance values of the same converter arm.

3) Effect of Parameter Spread: Thus far, the main assumption has been that all dc-capacitors exhibit equal parameters, specifically, that their capacitance and ESR values are the
Figure 5. (a) Capacitor conduction losses, and (b) temperature variation of all \( N = 20 \) submodule capacitors of an SPMMC when the converter load is changed from 0.2 p.u. to 1 p.u. and back. All capacitor ESRs are assumed to be the same.

Figure 6. Direct capacitance estimation of all \( N = 20 \) submodule capacitors of an SPMMC when the converter load is changed from 0.2 p.u. to 1 p.u. and back. All ESRs are given the same value. (a) No temperature correction, and (b) with temperature correction using (15). The black line in (a) shows the average of all estimated capacitance values in one arm.

Figure 7. (a) Capacitor conduction losses, and (b) temperature variation of all \( N = 20 \) submodule capacitors of an SPMMC when the converter load is changed from 0.2 p.u. to 1 p.u. and back. The ESR of all capacitors are different, ranging from -10\% to +10\% equidistantly.

In practice, the aforementioned parameters may be different, even in capacitors provided by the same manufacturer. For high-power MPPF capacitors, a typical design tolerance of \( \pm 10\% \) is expected. Hence, in this section, the ESRs of all capacitors are chosen to have an equidistant distribution within the \( \pm 10\% \) range. Difference in the initial capacitance values do not affect the simulation results as all estimated capacitance values are per-unitized using their initial capacitance. Simulation results for online estimation of the modified capacitors are shown in Fig. 7 and Fig. 8. In Fig. 8, it is evident that even considering the possible differences in ESRs, the method of comparing the capacitance deviation of each cell to the average deviated value remains effective in reducing the SoH estimation error. In these simulations, it is assumed that the capacitors have the same temperature coefficient and the same thermal capacity. Due to the similar size and mass of these modules, it is reasonable to expect that they have similar thermal capacitance. It has also been experimentally verified in Section V that the capacitors initially have a similar temperature coefficient. If this coefficient changes in a capacitor as a result of degradation, it will result in a drift of its capacitance compared to the average of all capacitance values, and can indicate an issue with the capacitor’s health. The proposed estimation algorithms have been proven to be equally accurate under various loads, different switching frequencies, and under various levels of measurement noise [17]. Hence, those studies are not repeated in this paper.

V. EXPERIMENTAL RESULTS

The proposed temperature compensation algorithm is applied to an SPMMC consisting of three full-bridge submodules. The experimental setup is shown in Fig. 9 and the main parameters of the hardware setup are summarized in Table II.
Figure 8. Direct capacitance estimation of all $N = 20$ submodule capacitors of an SPMMC when the converter load is changed from 0.2 p.u. to 1 p.u. and back. The ESR of all capacitors are different, ranging from -10% to +10% equidistantly. (a) No temperature correction, and (b) with temperature correction using (15). The black line in (a) shows the average of all estimated capacitance values in one arm.

Table II

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid voltage, peak</td>
<td>$V_g$</td>
<td>30</td>
<td>V.</td>
</tr>
<tr>
<td>Nominal load current, peak</td>
<td>$I_{arm}$</td>
<td>10</td>
<td>A</td>
</tr>
<tr>
<td>Nominal cell capacitance</td>
<td>$C_{cell}$</td>
<td>560</td>
<td>$\mu$F</td>
</tr>
<tr>
<td>Number of capacitor cells per submodule</td>
<td>$N_{ccpm}$</td>
<td>7</td>
<td>-</td>
</tr>
<tr>
<td>Number of submodules</td>
<td>$N_{cells}$</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>Arm inductance</td>
<td>$L_{arm}$</td>
<td>5</td>
<td>mH</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>$f_c$</td>
<td>711</td>
<td>Hz</td>
</tr>
</tbody>
</table>

A. Offline Capacitance Measurement at Different Temperatures

The capacitor bank of each submodule comprises seven parallel-connected aluminum electrolytic capacitors. The capacitance and ESR of each capacitor bank is measured using the BK Precision 895 RLC meter. The capacitance measurements are conducted at a measurement frequency of $f_m = 100\text{Hz}$. Offline measurements are repeated for all submodule capacitors at five different temperatures spanning from 20°C to 90°C. To conduct the measurements at different temperatures, the capacitors are placed in the Binder FP115 heating chamber as shown in Fig.10. At each temperature, the submodule capacitors are given one hour of time to reach thermal equilibrium. The temperature is monitored using a T-type thermocouple that has an accuracy of $\pm0.5^\circ\text{C}$. Moreover, temperature logging has been carried out using the Picolog TC-08. The offline measurements of the capacitance and ESR are shown in Fig. 11(a) and Fig. 12(a), respectively. Unlike MPPF capacitors, the capacitance of aluminum electrolytic capacitors has a positive temperature coefficient, resulting in an increase of capacitance at higher temperatures. The difference of capacitance and ESR to the average value at each temperature is calculated as

$$c_{\text{diff},i} = \left(\frac{c_i}{\sum_{j=1}^{N} c_j/N} - 1\right) \times 100$$

and

$$ESR_{\text{diff},i} = \left(\frac{ESR_i}{\sum_{j=1}^{N} ESR_j/N} - 1\right) \times 100,$$

and plotted in Fig. 11(b), and Fig. 12(b), respectively. It can be observed that the spread of capacitance to the average value at all temperatures is in the $\pm0.6\%$ range. Moreover, this difference does not vary significantly over the measured temperature range. Hence, the capacitance of all submodules have a similar temperature coefficient. The ESRs of this specific aluminum electrolytic capacitor show a nonlinear behaviour when subject to temperature changes. Nevertheless, the ESRs also have a similar temperature coefficient, and the spread of ESR compared to their average value at each temperature is less than 10%. Such spreads had been shown in Section IV-B2 to only create minor temperature imbalances. Hence, the estimation algorithms proposed in Section IV-B2 can be applied to this system.
Figure 10. Heating of submodule capacitors for conducting experiments at variable temperatures. Three submodule capacitors are placed in the Binder F115 heating chamber.

Figure 11. a) Offline capacitance measurement of submodule capacitor #1 (blue, o), submodule capacitor #2 (red, *), and submodule capacitor #3 (yellow, △) at different temperatures. b) Difference in capacitance of each submodule capacitor compared to their average value according to (16).

Figure 12. a) Offline ESR measurement of submodule capacitor #1 (blue, o), submodule capacitor #2 (red, *), and submodule capacitor #3 (yellow, △) at \( f_m = 1 \text{kHz} \) and at different temperatures. b) Difference in ESR of each submodule capacitor compared to their average value according to (17).

Figure 13. Online capacitance estimation of a submodule capacitor at different phase shifts of the modulating carrier signal. In each experiment, the carrier signal is phase-shifted by 45 degrees.

B. Online Capacitance Estimation at Different Carrier Phase Shifts

In the first experiment, the capacitance of the same module is estimated at different phase shifts of the modulating carrier signal, while the carrier signal of the other two submodules are kept the same. The entire system is kept at room temperature. The results are summarized in Fig. 13 and Fig. 14. This shows that the estimated capacitance is not affected by the carrier phase shift. Consequently, if this specific capacitor is placed in any of the submodules, the same capacitance value is estimated. The estimation error in all experiments are less than 0.5% after 1 second of estimation (or for \( N_{per} \geq 50 \)). The experimental results depicted in this paper show a sampling rate of one estimation per fundamental period. This is solely for demonstration purposes, and much slower sampling rates can be opted in practice. Based on the experimental results, the sampling rate should be one sample per second, or slower, to assure accurate estimations.

C. Loss Distribution

The conduction loss in each submodule capacitor is governed by (12). Assuming that the ESR of all submodule
D. Online Capacitance Estimation at Different Temperatures

In the second set of experiments, the capacitor banks are placed in the heating chamber, while the remainder of the system is kept at ambient temperature. The temperature of the chamber is varied, and for each variation, at least one hour is allowed for thermal equilibrium to be reached. Although reaching thermal equilibrium is not a requirement for the validity of the proposed estimation method, it is the only way of having a fair comparison between offline and online measurements. The online estimations are conducted sequentially for each submodule and are depicted in Fig. 16. The summary of the results, including comparison with offline measurements, are shown in Fig. 17(a). The accuracy of online estimations compared to offline measurements are summarized in Table III. The largest error between online and offline measurements is less than 1%. The compensated online estimations using (15) are shown in Fig. 17(b). The estimated SoH values using the proposed compensation method do not vary as a result of average temperature change in all submodule capacitors. Consequently, the proposed comparative algorithm can effectively mitigate the effects of temperature-induced fluctuations in submodule capacitance within an online configuration.

VI. CONCLUSION

In this paper, a unique algorithm is proposed for increasing the accuracy of online capacitance estimation in modular multilevel converters. The proposed algorithm can effectively separate temperature-related fluctuations in the estimated capacitance from degradation-related variations of the same by comparing the estimated capacitance of all submodule capacitors in each arm. The comparative method facilitates online condition monitoring by identifying outliers to the average expected capacitance in the each arm. The proposed solution does not require temperature sensors, and can be applied to a wide range of modular multilevel converter systems. Simulation and experimental results show that the capacitance- and therefore, the health state- of all submodule capacitors can be estimated with a maximum error of 1%, even under various temperatures of the submodule capacitors.

REFERENCES

Table III

<table>
<thead>
<tr>
<th>Measurement temperature [°C]</th>
<th>Offline measurement error for $c_1$ [%]</th>
<th>Offline measurement error for $c_2$ [%]</th>
<th>Offline measurement error for $c_3$ [%]</th>
<th>Offline measurement of $c_1$ [mF]</th>
<th>Offline measurement of $c_2$ [mF]</th>
<th>Offline measurement of $c_3$ [mF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>19</td>
<td>0.05</td>
<td>0.10</td>
<td>−0.01</td>
<td>3.57</td>
<td>3.55</td>
<td>3.55</td>
</tr>
<tr>
<td>30</td>
<td>0.05</td>
<td>0.03</td>
<td>−0.01</td>
<td>3.57</td>
<td>3.58</td>
<td>3.58</td>
</tr>
<tr>
<td>50</td>
<td>0.03</td>
<td>0.10</td>
<td>−0.01</td>
<td>3.65</td>
<td>3.63</td>
<td>3.63</td>
</tr>
<tr>
<td>70</td>
<td>0.10</td>
<td>0.10</td>
<td>−0.01</td>
<td>3.71</td>
<td>3.69</td>
<td>3.69</td>
</tr>
<tr>
<td>90</td>
<td>−0.01</td>
<td>−0.01</td>
<td>−0.01</td>
<td>3.76</td>
<td>3.75</td>
<td>3.75</td>
</tr>
</tbody>
</table>

Figure 16. Online capacitance estimation at different temperatures for submodule capacitor #1 (blue, o), submodule capacitor #2 (red, *), and submodule capacitor #3 (yellow, △).

Figure 17. a) Comparison of online capacitance estimation (solid) and offline capacitance measurements (dashed) at different temperatures for submodule capacitor #1 (blue, o), submodule capacitor #2 (red, *), and submodule capacitor #3 (yellow, △). b) Temperature compensation of online capacitance estimations using (15).


