Evaluation of SiC MOSFET Key Parameters for Nanosecond Pulsed Field Ablation: Investigating Discrepancies Between Experimental Data and Manufacturer Datasheet Values

Kai Zhu 1, Fukun Shi 1, Yuyi Guo 1, Jinling Gong 1, Junfeng Rao 1, and Jie Zhuang 1

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Abstract

Nanosecond pulsed field ablation (nsPFA) is a promising modality for clinical tissue ablation. The performance of the pulse generator (PG) strongly depends on the switching characteristics of the SiC MOSFET. Currently, many key parameters listed in SiC MOSFET datasheets are determined using double-pulse test circuits with inductive loads, whereas loads in nsPFA-applications are predominantly resistive. This study proposes a test scheme for SiC MOSFETs under nsPFA-like operating conditions. Key parameters to be evaluated are pulsed drain current (I_{DM}), on-resistance (R_{on}), rise/fall time, turn-on/off delay, and minimum pulse width. The results show significant differences between manufacturer datasheet values and experimental data. For example, one switch under test has an Idm value of 40 A in the datasheet but 153 A in experimental test. This study recommends that custom testing of SiC MOSFETs is essential when designing PGs for nsPFA-applications.
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Abstract— Nanosecond pulsed field ablation (nsPFA) is a promising modality for clinical tissue ablation. The performance of the pulse generator (PG) strongly depends on the switching characteristics of the SiC MOSFET. Currently, many key parameters listed in SiC MOSFET datasheets are determined using double-pulse test circuits with inductive loads, whereas loads in nsPFA-applications are predominantly resistive. This study proposes a test scheme for SiC MOSFETs under nsPFA-like operating conditions. Key parameters to be evaluated are pulsed drain current \((I_{dn})\), on-resistance \((R_{on})\), rise/fall time, turn-on/off delay, and minimum pulse width. The results show significant differences between manufacturer datasheet values and experimental data. For example, one switch under test has an \(I_{dn}\) value of 40 A in the datasheet but 153 A in experimental test. This study recommends that custom testing of SiC MOSFETs is essential when designing PGs for nsPFA-applications.

Index Terms— Silicon carbide (SiC) MOSFET, Nanosecond pulsed field ablation, Nanosecond pulse generators, Switching characteristics.

I. INTRODUCTION

High-voltage nanosecond pulsed electric fields (nsPEFs), a novel physical agent, are considered the next-generation solution for pulsed field ablation (PFA) [1, 2]. Nanosecond pulse generators (nsPGs) are the key module of nsPFA medical devices. Firstly, nsPGs must meet regulatory standards, encompassing stability, reliability, electrical safety, and EMC compliance [3]. Additionally, nsPGs should meet the specific requirements of tissue ablation, including high voltage (~10 kV) and high current (~100 A), along with fast pulse edges (typically less than 100 ns) [4, 5]. Furthermore, key output parameters, such as voltage, polarity, frequency and pulse width, should be accurately configured and offer a broad range of continuous adjustability. Unfortunately, there are few nsPGs available on the market that fulfill all of these requirements.

In the early 21\textsuperscript{st} century, most nsPEF biomedical researchers worked with nsPGs based on the pulse forming network (PFN) principles, controlled by spark gap switches [4, 6]. With the development of power semiconductor switching technology, all-solid-state PGs with semiconductor switches have become a mainstream solution for nsPEF research and product development [7]. It enables precise configuration and wide-range adjustment of various pulse parameters [8, 9]. Besides, the all-solid-state PGs offer high stability, extended operating life, and low electromagnetic interference [10, 11]. However, early silicon-based semiconductor switches, with either limited current capability (Si-MOSFET) or slower switching speed (IGBT), faced challenges in meeting the performance requirements of clinical nsPFA [5, 12, 13].

Recently, advancements in SiC MOSFET technology have opened up new opportunities for the R&D of nsPGs [7]. SiC MOSFETs present numerous advantages over Si-MOSFETs and IGBTs, including higher voltage ratings, higher current ratings, faster switching speeds, lower conduction losses and higher temperature operation [14, 15]. These features position SiC MOSFETs as promising candidates for the development of nsPGs for nsPFA applications. For instance, E. Pirc et al. designed a nsPG utilizing a series topology of SiC MOSFETs, producing ±4 kV pulses with a theoretical maximum current of 131 A and a minimum pulse duration of 200 ns. The in vivo ablation efficacy of this nsPG was evaluated in a mouse tumor model [16]. Based on the Marx topology, W. Zeng et al. developed a nsPG using SiC MOSFETs, achieving a voltage amplitude of up to ±10 kV with pulse widths ranging from 500 ns to 5 μs [8].

Presently, a wide variety of SiC MOSFETs are available on the market from different manufacturers, exhibiting a broad range of parameters and notable differences. The selection of a SiC MOSFET with suitable performance is essential for nsPG design in nsPFA applications. Nonetheless, most of the key parameters of SiC MOSFETs in the datasheet are obtained using the double-pulse test with inductive loads, which is significantly different from the operating conditions of nsPFA [17]. Specifically, the biological loads primarily exhibit resistive characteristics [18]. Additionally, there is a significant disparity in the voltage and current phases applied to SiC MOSFETs between the double-pulse test and the nsPFA-application process. To address this variance, Z. Ma et al. conducted a comprehensive study on the switching process and

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switching loss of SiC MOSFETs with resistive loads [19]. In addition, the pulsed drain current ($I_{\text{DM}}$) under pulsed conditions is theoretically calculated in certain datasheets [20, 21]. In short, depending on manufacturer’s datasheets to select suitable SiC MOSFETs for nsPFA-applications may yield misleading outcomes [19, 22]. However, studies on the selection and performance analysis of SiC MOSFETs for nsPFA-applications have been scarce.

The primary objective of this study is to develop a test scheme that can provide a theoretical basis and technical means for the optimal selection of SiC MOSFETs when designing nsPFA-applications. Another goal is to examine the applicability of the key parameters in the datasheet when the SiC MOSFETs are operated under npFA-like working conditions. To this end, a test circuit was designed with capacitor discharge topology, and six mainstream SiC MOSFETs with similar performance were evaluated. The evaluation involves various performance parameters relevant to npFG design, such as $I_{\text{DM}}, R_{\text{on}},$ rise/fall time, turn-on/off delay, and the minimum pulse width. To further validate the test results, npFA experiments were conducted on potato tissue samples. The experimental results reveal notable disparities in specific key parameters between datasheet values and experimental data under npFA-like operating conditions. The findings of this study may provide new insights into the selection of suitable SiC MOSFETs for the development of npFGs in npFA-applications.

II. EXPERIMENTAL DESIGN AND ANALYSIS

A. Design of the Test Circuit

To investigate the switching characteristics of SiC MOSFETs in npFA-applications, a test circuit is designed based on a capacitor discharge topology widely used in npFGs. The schematic circuit design is shown in Fig. 1(a), where $S_1$ and $S_2$ are SiC MOSFETs. $S_1$ is used to isolate the influence of the DC supply, while $S_2$ represents the selected switch under test. The drive voltage, $V_{\text{drive}}$, is generated by an FPGA (EP4CE10, Altera, UK, with 50MHz clock) through a driving chip (IXDN609, IXYS, USA).

The capacitor discharge circuit works as follows. Firstly, $S_1$ is turned on and $S_2$ is turned off. The DC supply ($V_{\text{dc}}$) (HSPY-1000-1A, Hanshengpuyuan, China) charges capacitor $C_j$ through $R_j$. After $C_j$ is fully charged, $S_1$ is turned off. Then, $S_2$ is switched on and off to generate pulses over load $Z_d$.

To accurately measure the on-state drain-source voltage, $V_{\text{ds(on)}}$, of $S_2$, a loop consisting of diode $D_j$, resistor $R_j$, and capacitor $C_2$ in parallel with $S_2$ is set. During the test, $C_2$ is charged to $V_j$. Before $S_2$ turns on, the drain potential of $S_2$ is higher than $V_j$, $D_j$ is cut-off, and $V_{\text{ds}}$ equals $V_j$. After $S_2$ turns on, the drain potential of $S_2$ is lower than $V_j$, $D_j$ is turned on, and $V_{\text{ds}} = V_j + V_{\text{ds(on)}}$. $V_j$ is measured by a high-precision low-voltage probe (PVP2350, RIGOL, China). Two high-voltage probes (CP-3308R, PINTECH, China), and a current monitor (Model 101, Pearson Electronics, USA) are used to measure drain-source voltage ($V_{\text{ds}}$), load voltage ($V_L$) and drain current ($I_d$) ($I_{\text{load}} = I_{\text{Load}}$). All waveforms are acquired with a digital oscilloscope (RIGOL, China) with 200MHz bandwidth and 1GS/s sampling frequency.

Fig. 1. The schematic design and equivalent circuit of the test platform
(a) The complete test circuit. (b) The parasitic elements in the main test loop.

B. Analytical Model of SiC MOSFETs

For a switch in the test circuit, waveforms of drive voltage ($V_{\text{drive}}$), gate-source voltage ($V_{gs}$), drain current ($I_d$), and drain-source voltage ($V_{ds}$) are illustrated in Fig. 2. During the time course of switching, the turn-on process is from $t_0$ to $t_1$, while the turn-off process is from $t_2$ to $t_f$.

The switching process of a SiC MOSFET in the test circuit with a resistive load can be divided into seven stages. Fig. 3(b) to (e) illustrate the operational states of the circuit at different stages, where red arrows indicate the direction of current flow within the loop.

1) Stage I ($t_0$–$t_1$), Fig. 3(b):

At time $t_0$, $V_{\text{drive}}$ transits from $U_{\text{g(off)}}$ to $U_{\text{g(on)}}$, initiating the charging of the switch’s gate-source capacitance ($C_{gs}$, $C_{gd}$). During this stage, the switch is in the off state. Due to the significant difference in capacitance ($C_{gs} >> C_{gd}$), charging of $C_{gd}$ can be ignored. According to Kirchhoff’s voltage and current laws, the basic circuit equations in the gate driving circuit can be expressed as follows:

$$V_{gs} = U_{g(on)} - \left[ I_g \cdot R_g + \frac{dI_g}{dt} \left( L_g + L_s \right) \right]$$

$$I_g = C_{gs} \frac{dV_{gs}}{dt}$$

2) Stage II ($t_1$–$t_2$), Fig. 3(c):

...
At time $t_1$, when $V_{gs}$ reaches the gate threshold voltage ($U_{th}$), the switch enters the saturation region and begins to turn on. $V_{drive}$ charges $C_{gs}$ and $C_{gd}$. $C_1$ discharges through the switch to $R_{load}$. $C_{ds}$ discharges through the switch as well. $I_d$ starts to increase, and $V_{ds}$ rapidly decreases. The circuit equations in the main test loop are as follows:

$$V_{gs} = U_{g(on)} - V_{R} - V_{t_x} - V_{L} = U_{g(on)} - \left[ I_g \cdot R_L + \frac{dI_g}{dt} \cdot L_g + \left( \frac{dI_g}{dt} + \frac{dI_d}{dt} \right) \cdot L_y \right]$$

$$U_{dc} = V_{ds} + \frac{dI_d}{dt} \cdot \left( L_y + L_d + L_{line} \right) + \frac{dI_g}{dt} \cdot \left( L_y + L_g \right) + R_{load} \cdot I_d$$

$$I_g = I_{gs} + I_{gd} = C_{gs} \cdot \frac{dV_{gs}}{dt} + C_{gd} \cdot \frac{dV_{gd}}{dt}$$

$$I_{C_{ds}} = -C_{ds} \cdot \frac{dV_{ds}}{dt}$$

$$I_{channel} = I_{gd} + I_d + I_{C_{sh}}$$

$I_{channel}$ refers to the total current flowing through the switch. Since the switch operates in the saturation region, $I_{channel}$ is controlled by $V_{gs}$:

$$I_{channel} = k \cdot (V_{gs} - V_{th})^2$$

Here, $k$ is a coefficient determined by the structure and material properties of SiC MOSFET.

3) Stage III ($t_2$–$t_3$), Fig. 3(d):

At time $t_2$, $V_{ds}$ decreases to $V_{gs} - U_{th}$, reaching the boundary between the saturation and ohmic regions. The switch enters the ohmic region, and $V_{gs}$ rises rapidly. During this stage, the turn-on process continues, and the current flow in the circuit is similar to Stage II. According to (5), due to the significantly larger $C_{gs}$ compared to $C_{gd}$ and the similar rate of change between $V_{gs}$ and $V_{gd}$, the charging current of $C_{gd}$ can be neglected.

4) Stage IV($t_3$–$t_4$), Fig. 3(e):

At time $t_3$, the switch is in complete conduction. $V_{gs}$ rises to $U_{g(on)}$. $V_{ds}$ decreases to $U_{drive(on)}$, and remains constant. $I_d$ reaches a steady state, given by:

$$I_d = \frac{U_{dc} - U_{ds(on)}}{R_{Load}}$$

5) Stage V($t_4$–$t_5$), Fig. 3(f):

At time $t_4$, $V_{drive}$ transits from $U_{g(on)}$ to $U_{g(off)}$, starts discharging switch gate ($C_{gs}$). The switch operates in the ohmic region. $V_{gs}$ begins to decrease, and $V_{ds}$ starts to rise. Similar to Stage III, the discharge current of $C_{gd}$ can be neglected during this process.

6) Stage VI($t_5$–$t_6$), Fig. 3(g):

At time $t_5$, $V_{ds}$ rises to $V_{gs} - U_{th}$, reaching the boundary between the saturation region and the ohmic region. The switch returns to the saturation region. $V_{drive}$ discharges $C_{gs}$. Energy storage capacitor $C_1$ charges $C_{ds}$ and $C_{gd}$ through $R_{load}$. $I_d$ starts to decrease, and $V_{ds}$ rises rapidly. This stage is similar to Stage II. (3), (4), (5), (6), and (8) still apply. And (7) transform to:

$$I_{channel} = I_d - I_{C_{sh}} - I_{gd}$$

The process of $C_1$ charging $C_{ds}$ through $R_{load}$ forms a second-order RLC series circuit.

$$\frac{d^2V_{ds}}{dt^2} + \frac{R_{Load}}{L_{loop}} \frac{dV_{ds}}{dt} + \frac{1}{LC_{ds}} \cdot V_{ds} = \frac{1}{LC_{ds}} \cdot U_{dc}$$

Here, $L_{loop} = L_s + L_d + L_{line}$.

Under the condition of underdamping ($\sqrt{L_{line}/C_{ds}} < 2R_{load}$), $V_{ds}$ will experience overshoot oscillations, with the oscillation angular frequency given by:

$$\omega_d = \sqrt{\frac{1}{LC_{ds}} - \frac{R_{load}^2}{2L_{loop}^2}}$$

7) Stage VII($t_6$–$t_7$), Fig. 3(h):

At time $t_6$, $V_{gs}$ decreases to $U_{th}$, placing the switch in the cutoff region. $V_{drive}$ continues to discharge $C_{gs}$. This stage resembles Stage I, but with reversed current flow, and equations (1) and (2) remain valid. At $t_7$, $V_{gs}$ drops to $U_{g(off)}$, concluding the turn-off process.

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Fig. 3. The simplified circuit of SiC-MOSFET and the working state in different stages

(a) The simplified circuit (b) Stage I ($t_0$–$t_1$) (c) Stage II ($t_1$–$t_2$) (d) Stage III ($t_2$–$t_3$) (e) Stage IV($t_3$–$t_4$) (f) Stage V($t_4$–$t_5$) (g) Stage VI($t_5$–$t_6$) (h) Stage VII($t_6$–$t_7$)

In the aforementioned process, Stage II determines the rise time of the switch. According to (8), the current flowing through the switch in the saturation region ($I_{channel}$) is primarily controlled by $V_{gs}$. $V_{gs}$ represents the voltage of $C_{gs}$, during the charging process of $C_{ds}$ and $C_{gd}$ by $V_{drive}$. Based on the relationship between voltage and current in capacitive components:
\[ u(t) = u(t_0) + \frac{1}{C} \int_{t_0}^{t} i d \xi \]  

(13)

\[ C_{gs}, C_{gd}, \text{and} \ I_g \text{ all influence the rise time.} \]

Stage VI, \( V_{drive} \) only discharges \( C_{gs} \), and \( C_{gd} \) is charged by \( C_t \). But the negative feedback circuit described in (14) still holds. Additionally, in Stage VI, there is a process where \( C_t \) charges \( C_{ds} \) through \( R_{Load} \). According to (11) and (12), with a larger \( R_{Load} \), the oscillation frequency decreases, the charging time of \( C_{ds} \) increases, and the fall time of the switch also increases. If \( R_{Load} \) is further increased, the circuit will enter an over-damped state, further extending the fall time.

C. Selection of Candidate SiC MOSFETs

In this study, six SiC MOSFETs, from different manufacturers, C2M0160120D, C2M0080120D, AIMW120R035M1H, C3M0021120D, MSC025SMA120B, and NVHL020N120S, are selected. They have the same package (To-247-3) and rated drain-source voltage (1200 V). The first two SiC MOSFETs were utilized in the development of nSPGs for biomedical applications by L. M. Redondo et al. [23] and V. Novickij et al. [24]. The last four are a new generation of SiC MOSFETs, with lower \( R_{on} \) and similar performance. The key nSPFAR-related performance parameters are listed in Table I.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>SELECTED KEY PERFORMANCE PARAMETERS OF THE SIX SiC MOSFETs UNDER TEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model</td>
<td>C2M0160 120D</td>
</tr>
<tr>
<td>( I_g /A )</td>
<td>18</td>
</tr>
<tr>
<td>( I_{DM} /A )</td>
<td>40</td>
</tr>
<tr>
<td>( R_{on} \text{/m}\Omega )</td>
<td>160</td>
</tr>
<tr>
<td>( t_r /\text{ns} )</td>
<td>9</td>
</tr>
<tr>
<td>( t_f /\text{ns} )</td>
<td>14</td>
</tr>
<tr>
<td>( t_{on} /\text{ns} )</td>
<td>7</td>
</tr>
<tr>
<td>( t_{off} /\text{ns} )</td>
<td>14</td>
</tr>
<tr>
<td>Manufacturer</td>
<td>CREE</td>
</tr>
<tr>
<td>Cost</td>
<td>$8.33</td>
</tr>
</tbody>
</table>

D. The Design of SiC MOSFET Test Experiments

For SiC MOSFETs, \( I_{DM}, R_{on}, \) rise/fall time, turn-on/off delay, and the minimum pulse width are critical parameters in nSPFA-applications. Through our experiments, the variation in pulse width does not affect the edge of the pulse when the switch is fully turned on. Unless otherwise specified, a pulse width of 500 ns is used in this study. The \( L_{load} \) in the datasheets of the six switches ranges from 10 A to 80 A, which is adopted by this study. The test voltage in datasheet for SiC MOSFETs with a drain-to-source voltage of 1200 V is 800 V. Therefore, in this study, the charging voltage of the DC source, \( V_{dc} \), is set to 800 V. Besides, the gate resistor (\( R_g \)) is set to 2 \( \Omega \), and the \( V_{drive} \) is set according to the value recommended in the datasheet. Various non-inductance resistors are used as loads to test the performance of SiC MOSFETs. (a) Pulsed Drain Current (\( I_{DM} \))

During \( I_{DM} \) test, pulse widths are set as 200 ns, 300 ns, 500 ns, and 700 ns. When a pulse width is chosen, the load resistance is gradually reduced and the peak current is recorded. When the peak current no longer increases as the load resistance is further reduced, it is considered \( I_{DM} \). The initial resistance is 10 \( \Omega \) and is gradually reduced.

(b) Drain-Source On-State Resistance (\( R_{on} \))

During \( R_{on} \) test, the charging voltage \( V \) of capacitor \( C \) is set to 20 V. The test current is adjustable from 10 A to 80 A in 10 A increments. Instant \( R_{on} \) values are calculated by recording \( V \) and \( I \) in the main test loop. For 500 ns pulses, \( R_{on} \) is determined as the average value from 350 to 450 ns period, as follows:

\[ R_{on} = \frac{V_{drive} - V_{c1}}{I_d} \]  

(15)

(c) Rise/Fall Time (\( t_r, t_f \)) and Turn-On/Off Delay (\( t_{on}, t_{off} \))

The rise/fall time and turn-on/off delay tests are performed simultaneously. The rise time (\( t_r \)) and fall time (\( t_f \)) are determined as \( V \) changes from 10% to 90% during the turn-on and turn-off process. The turn-on delay (\( t_{on} \)) is the time between \( V \) rising to 10% and \( V \) falling to 90%. The turn-off delay (\( t_{off} \)) is the time between \( V \) falling to 90% and \( V \) rising to 10%. These definitions shown in Fig. 4(a) are identical to the datasheet.
Regardless of the pulse width, NVHL020N120SC1 variations in the of A commute. Experiments of parallel plate electrodes conducted 2 by (50%, 100 mm thick), in biomedical applications, potato tubers purchased from local supermarket were cut into 2-mm thick slices for nsPFA experiments. The experiment is conducted as follows: (1) place potato slices between two parallel plate electrodes (10 mm radius); (2) perform nsPFA treatment with 100 pulses of 500 ns, 10 Hz; (4) record I and V of the first pulse; (5) repeat above steps for each switch.

E. Statistical analysis

All the data were obtained from at least three independent experiments. Statistical analyses were performed using IBM SPSS Statistics 27. Significant differences are identified by Duncan’s new multiple range test with a confidence level at P < 0.05.

III. EXPERIMENTAL VERIFICATION AND RESULTS

A. Test Results of Pulsed Drain Current (I\text{DM})

In biomedical applications, a higher pulse current capability of a switch is beneficial to increase the output power of the nsPGs and reduce the risk of overcurrent failure. Fig. 5 shows the I\text{DM} measured for the 6 SiC MOSFETs at increasing pulse widths (200 ns, 300 ns, 500 ns, 700 ns).

As shown in Fig. 5, there are significant differences in I\text{DM} between different switches. Each switch exhibits substantial variations in I\text{DM} at different pulse widths. As the pulse width increases, an increase in I\text{DM} is observed for each switch. Regardless of the pulse width, NVHL020N120SC1 has a notably higher I\text{DM} compared to other switches. For instance, at a pulse width of 700ns, its I\text{DM} reaches 395 A, which is 3.8 times the rated I\text{d} in the datasheet. At this pulse width, the I\text{DM} of C2M0160120D is 8.5 times the I\text{d} in the datasheet.

B. Test Results of Drain-Source On-State Resistance (R\text{on})

In nsPFA-applications, reducing the output impedance is essential to improve the load driving capability of a nsPG. From this perspective, the R\text{on} of a SiC MOSFET is a key factor. Fig. 6 shows the R\text{on} of the six switches at different I\text{d} values ranging from 10 A to 80 A. C2M0160120D, C2M0080120D, and AIMW120R035M1H exhibit an increase in R\text{on} with the increase of I\text{d}. The other three switches, however, do not show significant changes in R\text{on}. Noteworthly, during the test process, V\text{ds(on)} of C2M0160120D becomes higher than V\text{t} (20 V) when I\text{d} ≥ 50 A. Therefore R\text{on} can only be obtained for I\text{d} ≤ 40 A.

C. Test Results of Rise/Fall Time (t\text{R}, t\text{F})

Fig. 7 shows the rise/fall time of the six switches as I\text{d} increases from 10 A to 80 A. The results in Fig. 7(a) indicate that the rise time of the switches increases as I\text{d} increases. It is worth noting that the rise time of several switches is significantly different from their datasheet values, even at same test current conditions. More details are given in Table II. For example, the rise time of C3M0021120D (27 ns) is significantly shorter than that of NVHL020N120SC1 (57 ns) in the datasheet. Nevertheless, the situation is reversed when tested at I\text{d} = 80 A.

Fig. 7(b) shows that the fall time of most switches under test first decreases and then increases as I\text{d} increases. Similar to the rise time, there are also discrepancies with the datasheet. For instance, NVHL020N120SC1 has a fall time of 11 ns in the datasheet, which is shorter than the 13 ns of MSC025SMA120B. However, the fall time of NVHL020N120SC1 (63 ns) becomes significantly longer than that of MSC025SMA120B (43 ns) when I\text{d} is 80 A.
Table II  
**COMPARISON OF RISE TIME BETWEEN THIS STUDY AND DATASHEET**  

<table>
<thead>
<tr>
<th>model</th>
<th>Rise Time (ns)</th>
<th>this study (I_d = 80 A)</th>
<th>this study (I_d same as I_load in datasheet)</th>
<th>datasheet</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2M0160120D</td>
<td>115±4.9</td>
<td>98±1</td>
<td>9 (I_load = 10 A)</td>
<td></td>
</tr>
<tr>
<td>C2M0080120D</td>
<td>85±1</td>
<td>74±1</td>
<td>22 (I_load = 20 A)</td>
<td></td>
</tr>
<tr>
<td>AIMW120R035M1H</td>
<td>115±1.6</td>
<td>29±1 (I_d = 20 A)</td>
<td>38.3±1 (I_d = 30 A)</td>
<td>32 (I_load = 25 A)</td>
</tr>
<tr>
<td>C3M0021120D</td>
<td>116±5</td>
<td>63±0.9</td>
<td>27 (I_load = 50 A)</td>
<td></td>
</tr>
<tr>
<td>MSCO25SMA120B</td>
<td>96±2.5</td>
<td>45±1.6</td>
<td>12 (I_load = 40 A)</td>
<td></td>
</tr>
<tr>
<td>NVHL020N120SC1</td>
<td>83±4.9</td>
<td>83±4.9</td>
<td>57 (I_load = 80 A)</td>
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</tbody>
</table>

Table III  
**COMPARISON OF FALL TIME BETWEEN THIS STUDY AND DATASHEET**  

<table>
<thead>
<tr>
<th>model</th>
<th>Fall Time (ns)</th>
<th>this study (I_d = 80 A)</th>
<th>this study (I_d same as I_load in datasheet)</th>
<th>datasheet</th>
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</thead>
<tbody>
<tr>
<td>C2M0160120D</td>
<td>43.7±0.9</td>
<td>19±1</td>
<td>14 (I_load = 10 A)</td>
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<tr>
<td>C2M0080120D</td>
<td>53±1</td>
<td>23±1</td>
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<tr>
<td>AIMW120R035M1H</td>
<td>96±0.9</td>
<td>39±1 (I_d = 20 A)</td>
<td>45.7±1 (I_d = 30 A)</td>
<td>28 (I_load = 25 A)</td>
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<td>C3M0021120D</td>
<td>81±1</td>
<td>50±2.5</td>
<td>25 (I_load = 50 A)</td>
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</tr>
<tr>
<td>MSCO25SMA120B</td>
<td>43±1</td>
<td>31±1</td>
<td>13 (I_load = 40 A)</td>
<td></td>
</tr>
<tr>
<td>NVHL020N120SC1</td>
<td>63±1.6</td>
<td>63±1.6</td>
<td>11 (I_load = 80 A)</td>
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</tbody>
</table>

D. Test Results of Turn-on/off Delay (t_{on}, t_{off})  

Fig. 8 presents the turn-on/off delay of the six switches as I_d increases from 10 A to 80 A. As shown in Fig. 8(a), the turn-on delays of the switches are almost unaffected by I_d. Among them, C2M0160120D exhibits the shortest turn-on delay, ranging from 8 to 9 ns, while MSCO25SMA120B has the longest turn-on delay, ranging from 18 to 20 ns. The experimental turn-on delay results for the six switches are generally consistent with the datasheet values.

As shown in Fig. 8(b), the turn-off delay of the switches decreases with increasing I_d at similar slope. Among the switches under test, C3M0021120D has the longest turn-off delay, while C2M0160120D has the shortest. The experimental results of the turn-off delay for the six switches are in good agreement with the datasheet values, even though the test conditions for different switches in the datasheets are different.

Fig. 8. The turn-on/off delay of the 6 SiC MOSFETs under test with I_d from 10 A to 80 A  
(a) Turn-On Delay. (b) Turn-Off Delay.

E. Test Results of Minimum Pulse Width (t_{min})  

Minimum pulse width is a key parameter of nsPGs and is primarily determined by the switches. Fig. 9(a) shows the V_{on} of NVHL020N120SC1 with I_d set to 80 A and drive signal widths of 140 ns, 160 ns, 180 ns, and 200 ns. The switch is fully turned on for drive signal widths greater than 180ns, but not for widths less than 160ns. It is worth noting that even though the switch is not fully turned on, V_{on} still shows a plateau at the bottom, suggesting that the turn-off delay may play a role. According to the datasheet, the t_{off} of NVHL020N120SC1 is 45 ns. As shown in Fig. 9(a), it takes 46 ns and 45 ns for V_{on} to rise from 0% (bottom plateau) to 10% with 140 ns and 160 ns drive signals, respectively. The experimental results are in good agreement with the datasheet. Therefore, the minimum pulse width determined experimentally is between 138 ns and 166 ns. The minimum pulse width calculated using (16) is 147 ± 0.94 ns, which corroborates the experimental results.

Fig. 9(b) shows the minimum pulse width of the six switches as I_d increases from 10 A to 80 A. The results show that higher I_d significantly increases the minimum pulse width. For instance, NVHL020N120SC1 has a minimum pulse width of 94 ns at 10 A, which increases to 147 ns at 80 A.

Fig. 9. Experimentally determined minimum pulse width  
(a) Waveforms of V_{on} (NVHL020N120SC1) at different drive signal widths  
(b) Minimum pulse widths of six SiC MOSFETs with I_d from 10 A to 80 A

F. Results of nsPEF Potato Ablation  

Ablation experiments are conducted on potato slices. The rise time, fall time and voltage amplitude of the output pulses are shown in Fig. 10. Statistical analysis indicates that NVHL020N120SC1, MSCO25SMA120B, and C2M0080120D have the shortest rise time, as shown in Fig. 10(a). This is
consistent with the test results in Table II. The fall time results in Fig. 10(b) are also in good agreement with the test results in Table III.

The voltage amplitude of the output pulses is a key parameter for nsPGs in nsPFA-applications. Fig. 10(c) shows that C2M0160120D and C2M0080120D generate lower voltage amplitudes than the other four switches at the same DC charging voltage of 800 V.

IV. DISCUSSION

nsPFA-applications require unique pulse characteristics such as short pulse width, high voltage/current and fast edges. The aim of this study is to explore a guideline for the selection of suitable SiC MOSFET switches for nsPFA-applications. A test circuit based on capacitor discharge topology was designed and six SiC MOSFETs were tested for their key parameters, including $I_{DM}$, $R_{on}$, rise/fall time, turn-on/turn-off delay and minimum pulse width. The results show that certain key parameters in the datasheet, measured by the double-pulse test, can become significantly different in nsPFA-applications.

The double-pulse test, using inductive loads, is an industry standard for evaluating the performance of SiC MOSFET switches [14, 17]. However, the operating environment of a switch in nsPFA-applications differs significantly from that of the double-pulse test. In nsPFA-applications, the inductive component of the biological load is typically negligible, while the resistive component is the dominant factor, on the order of 100 $\Omega$ [18]. First, the use of inductive loads leads to desynchronization of $I_d$ and $V_{ds}$, whereas $I_d$ and $V_{ds}$ are nearly synchronized for resistive loads [17, 19]. Second, with inductive loads, the rise and fall time of the switch is mainly influenced by $C_{ds}$ and $C_{gd}$ [25]. However, with resistive loads, in addition to the two capacitors mentioned, the parasitic inductance of the switch must also be considered. Third, there are significant differences between the operation of the switch in the double-pulse test and in nsPFA-applications. The double-pulse test uses two control signals. The first control signal is used to store energy in the inductive load. The pulse width of the control signal, along with the load inductance, determines the $I_d$ of the switch. The second control signal is used to test various parameters of the switch, including switching loss and switching rate [14]. However, in nsPFA-applications, each control signal triggers an in-phase voltage/current discharge from the capacitor to the load through the switch [7]. The capacitor discharge circuit employed in this study represents the fundamental building block of nsPGs in most nsPFA-applications [7, 8, 16]. For instance, F. Yu et al. used a capacitor discharge circuit to investigate the differences between a Si MOSFET and a SiC MOSFET [15]. Thus, the test circuit in this study can more accurately replicate the operating conditions of SiC MOSFETs in nsPFA-applications.

Nearly all leading SiC MOSFET manufacturers provide datasheets that calculate $I_{DM}$ based on heat generation and dissipation under a single pulse, with the minimum pulse width typically set at 10 $\mu$s [20, 21]. In other datasheets, $I_{DM}$ is derived by multiplying $I_d$ by an empirical factor, often set as 3 or 4. In nsPFA-applications, the switches typically operate with pulse widths in the range of hundreds of nanoseconds, significantly shorter than 10 $\mu$s. Moreover, the pulse frequency is often limited to a few Hz to avoid inducing undesired temperature rise in the ablation target [26, 27]. In such scenarios, the switch generates considerably less heat and experiences a lower temperature rise. Over the range of pulse widths examined, the $I_{DM}$ of all switches shows an increasing trend with increasing pulse width. This behavior is due to the limited test pulse width of a few hundred nanoseconds. $I_{DM}$ continues to increase as the test pulse width increases. For example, at a pulse width of 1.3 $\mu$s, the $I_{DM}$ of NVHLO20N120SC1 reaches 548 A, which is significantly higher than the 412 A in the datasheet. In short, it is inevitably difficult to evaluate the $I_{DM}$ of a SiC MOSFET for nsPFA-applications by relying solely on the datasheet.

All six switches exhibit a longer rise/fall time compared to the datasheet, under similar operating current. As mentioned above, voltage and current are in phase in this study. Consequently, the presence of parasitic inductance leads to an increase in the rise/fall time compared to the value in the datasheet measured by the double-pulse test [19]. In Fig. 7(a), the rise time of all switches increases with $I_d$. A similar observation has been reported by S. H. Song et al [22]. They confirmed that the rise time of SiC MOSFETs increases with increasing $I_d$ and exhibits a significant deviation from the datasheet values. This phenomenon can be explained by the fact that as the operational current increases, it inherently takes more time for the switch to fully turn on. Furthermore, as shown in Fig. 7(b), when $I_d$ increases from 10 A to 80 A, the fall time of most switches shows a tendency to first decrease and then increase. This is explained in the description of the factors that determine the fall time. On the one hand, the presence of parasitic inductance leads to an increase in the fall time as $I_d$ increases. On the other hand, during the turn-off process, the combination of $C_{ds}$ and $R_{load}$ forms a first-order RC zero-state response circuit which charges $C_{ds}$. The increase in $I_d$ from 10 A to 80 A corresponds to a decrease in $R_{load}$ from 80 $\Omega$ to 10 $\Omega$. This decrease in $R_{load}$ results in faster charging of $C_{ds}$, leading to a decrease in fall time. Therefore, $I_d$ is a critical factor influencing the rise/fall time of SiC MOSFETs in nsPFA-applications.

The minimum pulse width is a critical parameter for nsPFA. A narrower pulse width can substantially reduce muscle contraction and improve ablation uniformity [2, 28]. As shown in Fig. 10(a), increasing the current above 30 A significantly increases the minimum pulse width achievable by a single switch. Therefore, the use of parallel switches may be necessary for nsPFA-applications requiring narrower pulse widths, e.g., less than 100 ns, even if a single switch can meet the load current requirements.

The measurement results of SiC MOSFETs are further validated by performing nsPFA experiments on potato samples. Experimental results indicate that the shorter rise time switch produces pulses with faster rising and falling edges, as well as higher voltage amplitude on potato samples. Studies have shown that both the pulse edge [29] and pulse voltage [30] can have profound impacts on ablation outcomes.

V. CONCLUSION

This study introduces a test circuit based on capacitor discharge topology to examine critical parameters of SiC MOSFETs for nsPFA-applications, specifically $I_{DM}$, $R_{on}$.
rise/fall time, turn-on/off delay and minimum pulse width. Following theoretical analysis and experimental evaluation, our main findings demonstrate:

1) The widely used double-pulse test is inadequate to evaluate SiC MOSFETs for nsPFA applications.

2) SiC MOSFETs with comparable performance parameters in the datasheet may display disparate behavior in the capacitor discharge test circuit, necessitating independent testing.

3) The minimum pulse width of a SiC MOSFET can be estimated from the pulse edge characteristics and the turn-off delay.

To summarize, this study confirms that certain key parameters listed in manufacturer’s datasheet inadequately represent the true performance of SiC MOSFETs under nsPFA operating conditions. The proposed test platform facilitates reliable evaluation of SiC MOSFETs during designing nsPGs for nsPFA-applications.

REFERENCES


