A Direct Modularization Method for Multi-cell to Multi-cell Equalizer with Large Cell Count

Shimul Dam 1 and Vinod John 2

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Abstract

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Shimul K. Dam, Member, IEEE, and Vinod John

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Index Terms—Voltage equalizer, modular, fast balancing.

I. INTRODUCTION

THE voltage equalizer assumes a critical role in battery management systems in equalizing cell voltages within a battery stack. This equalization not only significantly enhances the utilization of stored energy but also extends the overall lifespan of the battery bank. While passive equalizers offer a simpler and cost-effective solution [1], [2], active equalizers present advantages such as high energy efficiency, less challenging thermal management, increased utilization of stored energy, and prolonged battery life [3]. The complexity of active equalizer topologies, however, prompts a need for a modular approach to avoid redesigning for different applications with different numbers of cells. The modular strategy, where a module equalizes a fixed small number of cells, and the number of modules is varied based on the total cell count in an application, allows a standardized design across diverse applications. This approach facilitates mass production, yielding substantial cost savings. The process of modularizing a voltage equalizer introduces additional circuitry, potentially leading to a significantly increased cost and size. Therefore, a modularization method should have the following features,

1) The number of additional components for modularization and their cost should be low.

2) The electrical stresses on the equalizer components as well as additional components should be low, and should not increase with an increase in the number of modules.

3) The losses in the additional components should be low so that the overall efficiency is not impacted.

4) Inter-module charge transfer should be fast so that overall equalization speed is not reduced.

The available modularization methods in literature can be classified as: (a) double tier equalizer based [2], [4]–[13], (b) adjacent cell based [14]–[16], (c) multi-winding transformer based [17]–[22], and (d) individual cell transformer based approach.

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Fig. 1. Modularization methods: (a) double tier equalizer based, (b) adjacent cell based, (c) multi-winding transformer based, and (d) individual cell transformer based approach.

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of the next module. Since the additional equalizer is always connected between two adjacent cells, its cost is lower and its design does not change with the number of modules. However, this method does not allow direct charge transfer from non-terminal cells of a module, leading to a low speed of inter-module equalization. For this reason, its application is usually limited to lower-speed adjacent cell equalizers [14]–[16].

Multi-winding transformer based modularization [17]–[22] is used when the cells of a module are equalized using a multi-winding transformer based equalizer. Each cell is connected to one winding of the transformer. An additional winding is added to the multi-winding transformer for modularization purpose. The additional windings from all the modules are then connected together, as shown in Fig. 1(c), to achieve power flow among modules. This method has minimal additional cost and the ratings of all the component ratings are independent of the number of modules.

Individual cell transformer based modularization method can be realized in equalizer topologies, where each cell has its own transformer [23]–[25]. These are isolated converter based equalizers, in which the transformer secondary windings are either directly connected or rectified and connected to a common DC link, allowing a direct power flow path from any cell to any cell. Modularization is achieved here by connecting the common secondary bus of each module together, as shown in Fig. 1(d). Thus, this method also has a minimal additional cost for modularization, and equalizer component ratings do not change with the number of modules. However, individual transformers require almost twice the number of windings compared to multi-winding transformer based equalizers. This drawback is addressed in [26], [27] by using one transformer for two cells. Thus, the benefit of simple modularization is retained using the same number of windings as the multi-winding transformer topology.

From the discussion, it is observed that the transformer based equalizers offer simple and low-cost modularization that is independent of the number of modules and offers direct fast charge transfer paths among all the cells. However, the transformer based equalizers use multi-winding transformers or several two-winding transformers, leading to bulky magnetic and additional power loss. On the other hand, the transformer-less equalizers offer compact designs but do not offer simple modularization. Modularization of a transformer-less equalizer employs either double-tier modularization with increased cost and size, or adjacent cell modularization with slower equalization.

This work proposes a new modularization method using only one additional two-winding transformer per module of a transformer-less equalizer. This brings all the benefits of transformer based modularization while retaining the benefit of a transformer-less compact design at the inter-cell level. The proposed method has the following benefits,

1) Use of only one two-winding transformer per module ensures small additional cost and loss.
2) Electrical stresses on components are independent of the number of modules to avoid the need for redesign for different applications.
3) Direct charge transfer path from any cell(s) in one module to any other cell(s) in another module, ensuring fast equalization speed.
4) Modularized control structure, eliminating the need for controller redesign.

The details of the proposed modularization method are explained in Section II, utilizing a transformer-less equalizer [28]. Section III introduces a modularized control structure, while Section IV compares the proposed method with existing approaches. Experimental verification is conducted in Section V, followed by the conclusion.

II. PROPOSED MODULARIZATION METHOD

The proposed modularization method is explained with a transformer-less multi-cell to multi-cell topology shown in Fig. 2(a). This equalizer topology is selected due to its capability of equalizing all cells simultaneously and maintaining almost constant cell current levels throughout the equalization duration to achieve fast cell balancing [28]. It also has inherent soft-switching, allowing a high switching frequency design with small passives. The topology has a common inductor node through which energy can be transferred from multiple cells to multiple cells directly. The proposed modularization method is applicable to any transformer-less multi-cell to multi-cell topology which follows the same principle of exchanging energy through a common node like Fig. 2(a).

A. Operation and Control of Equalizer Module

The operating principle and control strategy of the equalizer in Fig. 2(a) are discussed in detail in [28] and summarized here. The equalizer has one half-bridge, two capacitors, and one inductor connected to each cell. The capacitors \( C_{dc1} \) and \( C_{i} \), where \( i \in [1, n] \), are used for AC current filtering and DC voltage blocking respectively. The inductors \( L_{i} \) are used for energy transfer. Each half bridge is controlled with a square-wave signal. All discharging half-bridges are controlled with the same signal \( S_{dis} \) and all charging half-bridges are controlled with another signal \( S_{ch} \). The signal \( S_{ch} \) lags \( S_{dis} \) by a predetermined phase that is selected to achieve the required
equalization current level. The peak current in inductor $L_i$ is given by [28],

$$I_{L(peak)} = \frac{(n-1)}{8nf_sL_f}(V_{b(max)} - (1 - 4\delta)V_{b(min)})$$  \hspace{1cm} (1)

where, $n$ is number of cells, $L$ is inductance, $f_s$ is switching frequency, $V_{b(max)}$ is maximum possible cell voltage, $V_{b(min)}$ is minimum possible cell voltage, and $\delta$ is the phase shift such that phase shift angle is $2\pi\delta$. The peak voltage stress on capacitors $C_{dc1}$ and $C_i$ are given by,

$$V_{C_{dc1}(max)} = V_{b(max)}, \quad V_{C_i(max)} = \frac{n-1}{2}V_{b(max)}$$  \hspace{1cm} (2)

The current and voltage stresses of the switches can also be obtained from (1) and (2) respectively. It can be observed that for a higher number of cells $(n-1) \simeq n$ and the peak current in (1) approaches a fixed value of $\frac{1}{8nf_sL_f}(V_{b(max)} - (1 - 4\delta)V_{b(min)})$.

Thus, a module designed for this peak current can be used in a cell stack of any number of cells. On the other hand, the voltage stress on $C_i$ in (2) increases proportionally with the number of cells with no upper limit. Thus, the maximum number of cells in an application must be known before the design of the equalizer. This requirement presents a difficult challenge in modular design.

**B. Modularization Method**

If $m$ number of $n$-cell modules in Fig. 2(a) are connected in series to equalize $m * n$ cells, it results in a proportional increase in voltage stress on the capacitors in (2) by a factor of $m$. Consequently, the $n$-cell module must be designed to withstand the worst-case voltage stress, taking into account the series connection of $m$ modules. However, if a different application necessitates a higher number of cells in series, requiring $m + 1$ modules, the same module design becomes invalid. To address this challenge, the proposed modularization method ensures that the module design remains independent of the number of modules, allowing for its application across a wide range of scenarios.

The proposed modularization method is explained using a four-cell example in Fig. 2(b). The series-connected filtering capacitors $C_{dc1}$ in Fig. 2(a) are rearranged in an equivalent star-connection in Fig. 2(b) to provide a common capacitor node $N_1$, which is then connected to cell stack mid-point. One transformer per module is needed for the proposed modularization method. The primary winding of the transformer is connected between $N_1$ and $N_2$. The connection of three 4-cell modules using the proposed modularization method is shown in Fig. 3. Inter-module connection is achieved by connecting the secondary windings of the modularization transformers together. The power flow among the cells in different modules can be explained with an AC equivalent circuit.

Based on the DC blocking capacitors, $C_{dc1}$ in Fig. 2(a), an AC equivalent circuit for the equalizer is derived in [28], and is shown in Fig. 4(a). The AC voltage sources in Fig. 4(a) represent the AC components of the pole voltages of the half-bridges. Similarly, an AC equivalent circuit for the modularized equalizer in Fig. 2(b) can be derived, a shown in Fig. 4(b). Due to the interconnection of the secondary windings in the modularization transformers, the equivalent circuit of the 3-module equalizer in Fig. 3 is derived in Fig. 5(a). The modularization transformer is constructed using bifilar winding on a toroidal core resulting in low leakage inductance. Consequently, the leakage inductances $L_{lk1}$ and $L_{lk2}$ are deemed negligible compared to inductors $L_i$. The magnetizing inductance on the other hand is large compared
to \( L_i \), and the magnetizing current at the switching frequency can be disregarded. By substituting the magnetizing inductance with an open circuit and neglecting the leakage inductances in Fig. 5(a), an equivalent circuit with an ideal transformer is obtained, as illustrated in Fig. 5(b).

Examining Fig. 5(b), it is evident that the equivalent circuit of three series-connected 4-cell equalizer modules is the same as that of a single 12-cell equalizer. Consequently, the power flow management and phase-shift control for multiple modules seamlessly extends from the control principles established for a single module in [28]. However, it will be demonstrated in the next section that the electrical stresses on the 4-cell module components do not increase when three modules are connected in series, with the proposed modularization technique.

C. Electrical Stresses on Components

The capacitors \( C_{dc1} \) and \( C_1 \) in the equalizer in Fig. 2(a) and (b) are designed to block DC voltage and have low AC ripple. Hence, their voltage stress is determined from the DC equivalent circuit of the equalizer. Since the half-bridges are controlled with a square wave modulation signal, the DC voltage generated at the pole is half of the cell voltage. The DC equivalent circuit of the 4-cell equalizer in Fig. 2(b) is derived in Fig. 6 by replacing the inductors and transformer winding with short-circuit and replacing the half-bridge with equivalent DC voltage source \( \frac{V_b}{2} \).

1) Capacitor Voltage Stress: By applying KVL in the DC equivalent circuit, the voltage stresses on the capacitors are,

\[
\begin{align*}
V_{C_{dc1}} &= \begin{bmatrix} \frac{V_b}{2} + V_{64} \\ \frac{V_b}{2} \end{bmatrix}, & V_{C_{dc2}} &= \begin{bmatrix} \frac{V_b}{2} + V_{62} \\ \frac{V_b}{2} + V_{63} \end{bmatrix}, \\
V_{C_{dc3}} &= \begin{bmatrix} \frac{V_b}{2} + V_{63} \\ \frac{V_b}{2} + V_{64} \end{bmatrix}, & V_{C_{dc4}} &= \begin{bmatrix} \frac{V_b}{2} + V_{62} \\ \frac{V_b}{2} + V_{64} \end{bmatrix}
\end{align*}
\]  

Hence, the worst-case voltage stress will be,

\[ V_{C_{dc2}} = 2V_{b_{\text{max}}}, \quad \text{and} \quad V_{C_{dc1}} = \frac{3}{2}V_{b_{\text{max}}} \]  

2) Inductor Current Stress: Since the AC equivalent circuit of the modularized equalizer in Fig. 2(c) is the same as that of a single-module equalizer in Fig. 2(a), the peak inductor current in modules of Fig. 2(c) is also given by (1) and upper bound of this peak current for any number of cells is obtained by assuming \((n - 1) \approx n\) and is given in (5).

\[ I_{L_{\text{pk}}} = \frac{1}{8L_f s} [V_{b_{\text{max}}} - (1 - 4\delta)V_{b_{\text{min}}}] \]  

3) Maximum Stress on Transformer: In the worst-case scenario, the transformer winding carries a sum of four inductor currents. Thus, the maximum possible current stress in transformer winding is given in (6). The modularization transformer is designed to withstand the maximum possible Volt-sec condition. From the AC equivalent circuit in Fig. 4(b) the voltage applied on transformer winding is average of \( v_1, v_2, v_3, \) and \( v_4 \). Since the AC voltage \( v_i \) is the AC component of pole voltage and the half-bridge is controlled with square wave signal, the waveform of voltage \( V_s \) is also a square wave of switching frequency and amplitude of \( V_{b_{\text{max}}} / 2 \). Thus, the peak voltage and the maximum Volts-sec of the transformer winding are given in (7).

\[ I_{L_{\text{t}}_{\text{pk}}} = \frac{1}{8L_f s} [V_{b_{\text{max}}} - (1 - 4\delta)V_{b_{\text{min}}}] \]  

4) Generalized Expressions of Stresses: The electrical stresses derived in previous sections are for a 4-cell module. In the case of \( m \) number of \( n \)-cell modules, the expressions for electrical stresses can be extended as follows,

\[ V_{C_{dc2}} = \frac{n}{2}V_{b_{\text{max}}}, \quad \text{and} \quad V_{C_{dc1}} = \frac{n - 1}{2}V_{b_{\text{max}}} \]  

\[ I_{L_{\text{t}}_{\text{pk}}} = \frac{1}{8L_f s} [V_{b_{\text{max}}} - (1 - 4\delta)V_{b_{\text{min}}}] \]  

\[ I_{T_{r}} = \frac{V_{b_{\text{max}}}}{2}, \quad V_{T_{r}} = \frac{V_{b_{\text{max}}}}{4L_f s} \]
It is evident from (7) and (8)-(10) that the electrical stresses on the equalizer components remain independent of the number of modules \( m \), and only depend on the number of cells in a single module \( n \). The isolation voltage between the primary and secondary windings of the transformer can be as high as the battery stack voltage, which can be up to a few hundred Volts for most applications. The standard wires employed for transformer windings are commonly engineered to withstand such voltages. Thus, a module designed for \( n \) cells can be used for \( m \times n \) cells, without changing the module design.

III. MODULARIZED CONTROL

The equalizer in Fig. 2 is controlled by a set of complementary pulses for all charging cells and another set of complementary pulses with lagging phase for all discharging cells. For a small number of cells in one module, all required gate pulses can be provided by a low-cost controller. However, for a large number of modules, the number of gate drive signals is too large for a low-cost controller. Thus, a modular control architecture is proposed in this work.

In the proposed modular decentralized control scheme, each module has its own low-cost controller. However, for proper operation, the pulses generated by the controllers should be synchronized. All controllers share the same signal ground. A common signal bus with voltage \( V_{\text{synch}} \) in Fig. 7 is utilized for synchronization. At power on, each controller actively monitors the voltage on the \( V_{\text{synch}} \) bus, attempting to detect any pulse signal over a switching period. If no pulse is detected, then the controller generates a switching-frequency square wave on \( V_{\text{synch}} \) bus, else it does not drive the \( V_{\text{synch}} \) bus. Once a pulse signal is present on the \( V_{\text{synch}} \) bus, each controller utilizes this signal as the leading-phase gate signal. It subsequently generates a lagging-phase signal by introducing a delay to the leading-phase signal.

The controller for the equalizer in Fig. 2 also needs to evaluate the average voltage of all the cells. To accomplish this, all the differentially sensed cell voltages are connected to a common signal bus with voltage \( V_{\text{avg}} \) through identical resistors \( R_a \), as shown in Fig. 7. Using the superposition theorem, it can be shown that the voltage \( V_{\text{avg}} \) represents the average of all the cell voltages. Each controller senses the cell voltages of its own module and the average cell voltage of the entire stack without communicating with other controllers. Consequently, the equalizer’s control is executed in a modular fashion, accommodating any number of modules seamlessly.

IV. COMPARISON WITH EXISTING METHODS

The effectiveness of the proposed modularization method is assessed in comparison to six other equalizers in Table I. The left segment of Table I scrutinizes the inter-cell equalizers within each module, while the right segment compares the performance and additional component requirements for modularization. The first equalizer [16] in Table I uses adjacent cell modularization, offering slower inter-module equalization speed. The second and third equalizers [10] and [8] utilize double-tier modularization to achieve faster inter-module equalization but with higher additional component count, resulting in increased cost and size. Despite using more components, these methods can not achieve direct cell to cell energy transfer among modules. The fourth equalizer [29] uses a lower number of passive components for modularization but is limited to slower adjacent cell modularization.

In contrast, the fifth and sixth equalizers in Table I demonstrate the ability to achieve rapid inter-module equalization with fewer [21] or no additional [9] passive components. This is possible due to their transformer based equalizer topologies with increased inter-cell equalizer complexity. The proposed modularization also uses a low number of passive components and achieves direct energy transfer from any cell(s) of one module to any cell(s) of another. It provides the benefits of simpler and faster modularization like [9], [21] with fewer total number of transformer windings for compact design. Unlike the equalizers in [8], [10], [29], the designs of the components of the proposed equalizer do not depend on the number of modules and can be seamlessly employed in various applications without necessitating redesign.

V. EXPERIMENTAL RESULTS

The proposed modularization method is experimentally validated using three 4-cell equalizer modules. Each module is designed to equalize four 3.6 V, 2.6 Ah Li-ion cells with an equalization current of 0.5 A. The designed module uses low-voltage MOSFETs and operates with a switching frequency of 100 kHz. The developed module prototype is shown in Fig. 8 and the ratings of major components are given in Table II.

When three modules are connected in series, they are interfaced with inter-module connectors. The gate drive signals for each module are generated by its own controller as shown in Fig. 8(c) to demonstrate the proposed decentralized control concept. The controller here is a FPGA board [30], which can be replaced with a low-cost controller. With a three-module setup, the operation and soft-switching of the equalizer are verified first, followed by verification of cell voltage equalization under rest, charging, discharging, and varying load conditions. The voltage stresses on different components are evaluated to demonstrate the effectiveness of the proposed modularization concept.

A. Validation of Soft-switching

The experiment verifies the ZVS (Zero Voltage Switching) transition. Given the compact nature of the prototype, direct
TABLE I
COMPARISON OF COMPONENT COUNT AND MODULARIZATION PERFORMANCE.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Requirements for $m$ number of $n$-cell modules</th>
<th>Requirements for inter-module equalization</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>For inter-cell equalization</td>
<td>For inter-module equalization</td>
</tr>
<tr>
<td></td>
<td>Required components</td>
<td>Required components</td>
</tr>
<tr>
<td></td>
<td>M*</td>
<td>C*</td>
</tr>
<tr>
<td>----------</td>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>[16]</td>
<td>$2nm$</td>
<td>$2nm$</td>
</tr>
<tr>
<td>[10]</td>
<td>$nm$</td>
<td>$nm$</td>
</tr>
<tr>
<td>[8]</td>
<td>$(2n+6)m$</td>
<td>$nm$</td>
</tr>
<tr>
<td>[29]</td>
<td>$2nm$</td>
<td>$2nm$</td>
</tr>
<tr>
<td>[9]</td>
<td>$4nm$</td>
<td>$(3n+2)m$</td>
</tr>
<tr>
<td>[21]</td>
<td>$2nm$</td>
<td>$2nm$</td>
</tr>
<tr>
<td>Proposed</td>
<td>$2nm$</td>
<td>$2nm$</td>
</tr>
</tbody>
</table>

*M: MOSFETs, C: capacitors, L: inductors, T: transformer windings; †The proposed modularization method uses inter-cell equalizer in [28].

![Image](image-url)

Fig. 8. (a) Front side and (b) back side of a four-cell voltage equalizer module prototype, (c) three-module voltage equalizer for 12 Li-ion cells.

TABLE II
CRITICAL COMPONENTS OF THE MODULE PROTOTYPE.

<table>
<thead>
<tr>
<th>Component</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET</td>
<td>BSC0911ND, 25V, 3.2 mΩ</td>
</tr>
<tr>
<td>DC blocking capacitors, $C_i$</td>
<td>6 x 10 μF, 50V</td>
</tr>
<tr>
<td>DC bus capacitors, $C_{bci}$</td>
<td>6 x 10 μF, 50V</td>
</tr>
<tr>
<td>Inductor, $L_i$</td>
<td>MSS1246T-102, 1 μH, 8 A</td>
</tr>
<tr>
<td>Transformer $T_{mod}$</td>
<td>1:1, 2.5 V, 8 A</td>
</tr>
</tbody>
</table>

Fig. 9. Experimentally observed voltage waveforms during (a) turn-on, (b) turn-off transitions of a half-bridge.

1) Test under Rest Condition: The first test is performed on 12 Li-ion cells at no-load condition. At the beginning, there is 390 mV unbalance among the cell voltages. The equalizer is then enabled and the cell voltages are balanced within a narrow band of 15 mV within 58 minutes, as shown in Fig. 10.

2) Test under Charge-discharge Cycle: In this test, the performance of the equalizer is evaluated under one complete charge-discharge cycle. All the cell voltages are unbalanced

B. Evaluation of Voltage Equalization Performance

The voltage equalization performance of the three-module equalizer is evaluated under three different circumstances.
3) Test with Varying Load: The cell stack is subjected to varying load currents of 0.5 C and 1 C for 10 minutes each followed by another cycle of the same load pattern. The cell voltages observed during this test are plotted in Fig. 12, which shows that the equalizer is effectively keeping the cell voltages within a narrow band of 15 mV during the loading cycles.

C. Voltage Stresses on Equalizer Components

For a maximum Li-ion cell voltage of 4.2 V, the theoretical voltage stresses for capacitor $C_i$, $C_{dci}$, and transformer $T_{mod}$ are calculated from (8) and (14) as 6.3 V, 8.4 V, and 2.1 V respectively. The observed voltage stresses on DC blocking capacitors $C_i$ and DC link capacitors $C_{dci}$ are shown in Fig. 13. The voltages applied on the transformer windings are shown in Fig. 14. The peak voltages observed in these waveforms are lower than the theoretical limits.

D. Efficiency Measurement

The efficiency is measured for rated load condition when all the twelve Li-ion cells connected to three equalizer modules are participating in equalization. During this test, six cells are discharging and six are charging. As each module has a rated power of 4 W, the efficiency of the three-module prototype is tested up to 12 W. The measured efficiency is plotted over the power in Fig. 15. It can be observed that the equalizer achieves a peak efficiency of 86.5% at 54% load and 84.6% at the rated load of 12 W.

VI. Conclusion

A new modularization method is proposed for a transformer-less equalizer that can achieve fast and simple inter-module equalization. The proposed modularization achieves direct energy transfer from any cell(s) in a module to any cell(s) in another module using only one two-winding transformer per module. The electrical stresses on the components of the equalizer as well as modularization transformer is shown to be independent of the number of modules, allowing the use of one design for a wide variety of application. A modularized control structure is proposed to enable design with module number independent control design. A comparison study is performed to show that the proposed equalization method is faster and/or has lower cost and size compared to existing modularization methods for transformer-less equalizers. The proposed concept is validated experimentally using three four-cell module prototype balancing 12 Li-ion cells with an efficiency of 84.6% at the rated power. The analytical derived module number independent component stress limits are verified experimentally and equalization performance is validated under different load conditions. In conclusion, the proposed modularization method not only delivers excellent equalization performance but does so with a design that is both compact and cost-effective.

REFERENCES

Fig. 13. Measured voltage stresses on DC blocking capacitors $C_i$ in (a) module 1, (b) module 2, (c) module 3 and voltage stresses on DC link capacitors $C_{dic}$ in (d) module 1, (e) module 2, (f) module 3.

Fig. 14. Measured voltage waveforms transformer primary windings in (a) module 1, (b) module 2, and (c) module 3 at overall equalizer power rating of 12 W.

Fig. 15. Measured efficiency curve of 12-cell 3-module prototype.


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