Digital-Like Built-In Defect-Oriented Test for Analog-Mixed Signal Circuits

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Abstract

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Index Terms—Analog and Mixed signal circuits, Defect-oriented Test, Built-In self-Test, Defect coverage, Analog-to-Digital converter.

I. INTRODUCTION

We continue to witness an increase in both the number and complexity of integrated circuits (ICs) being embedded in safety-critical applications, such as automotive systems. Remarkably, in the automotive industry alone, the number of ICs per vehicle has already surpassed the astonishing number of 400 ICs per vehicle [1]. This requires a more stringent approach to ensuring the reliability and functional safety of these embedded ICs. Certain automotive standards such as ISO-26262 and AEC-100, require near zero defective parts per million, (0 DPPM). In fact, for some of these devices, reliability and functional safety criteria might even outweigh the performance requirements. Furthermore, non-mission-critical applications are increasingly adopting similar reliability standards due to the higher expected lifetimes of these devices. Furthermore, non-mission-critical applications are increasingly adopting similar reliability standards due to the higher expected lifetimes of these devices. While achieving these stringent reliability standards is feasible through rigorous post-manufacturing tests to a certain extent [2]–[4], they offer no guarantee against in-field failures. Moreover, the varied environments in which these safety-critical ICs operate cannot be fully accounted for during post-manufacturing tests. It should also be emphasized that rigorous post-manufacturing tests are expensive endeavors, especially considering the cost-sensitive nature of the automotive semiconductor industry.

Therefore, system designers are increasingly compelled to employ built-in-self-test (BIST) solutions. This not only reduces testing time and costs but also significantly enhances the functional safety of ICs by enabling in-field health monitoring of the devices.

Based on the failure reports, nearly 80% of the in-field IC failures are due to malfunction in Analog and Mixed signal (AMS) circuits [5], [6]. Considering the fact that AMS circuits comprise only 20% of the area in a general SoC but are responsible for 80% of the failures, makes the functional safety and reliability concerns in AMS circuits even more critical [5]. This significant difference between reliability performance of the AMS circuitry and their digital counterparts primarily comes from the nature of AMS circuitry, making the development of structural tests for these circuits a challenging task.

Over the last few decades, several methods and strategies have been introduced, developed, and advanced for defect-oriented structural testing of the digital circuits. In addition, several standards have been developed to systemize these tests for digital circuits. However, AMS circuits have been and mostly still are, being tested only for characteristic performance. The lack of a systematic structural test for AMS circuits is largely due to the nature of these circuits. When a defect occurs in AMS circuits, it often results in only a slight deviation from the nominal expected value, which still falls within the desired, acceptable range and may be crossed out as the result of the process, voltage temperature (PVT) variation. However, in the long run, it is these seemingly innocuous defects that might result in a latent failure of the said circuit block or even the entire IC as the IC faces harsh environmental conditions in field. As an example, in the automotive industry, most in-field IC failures happen after thousands of kilometers of driving. Therefore, though structural defects in AMS circuitry may not significantly affect the IC’s characteristics initially, rendering them invisible during the characteristic testing, they need to be detected, nonetheless. This lack of structural test for AMS circuits and their impact on IC reliability has recently made defect-oriented testing for AMS circuits a hot topic [3], [7], [8], leading to the ongoing development of IEEE 2427 standard addressing this issue [9].

As mentioned, little research has been performed on developing structural defect-oriented tests for AMS circuits. Among the few, is SymBIST [10]. SymBIST, introduces a BIST based on the inherent or pseudo symmetries in a circuit that can generate values referred to as invariant. These invariants should fall within an acceptable, defect-free range;
any violation of this range indicates detection of a defect. The most important feature of this approach is the transparency of the BIST with respect to the main circuit. However, the approach is tested for a selected set of defects and has an overall average defect coverage of 87.56%. Another work is [11], in which the analog circuit is broken down into small circuits of operational amplifier (OA), comparators, phase lock loop (PLL), and filters. These subcircuits are then converted to oscillators by adding proper circuitry. Defects are detected by comparing the oscillation parameters with the nominal values. This work represents one of the early endeavors in AMS structural testing, providing a solution for AMS reliability concerns. However, it necessitates circuit alterations and the addition of resistive and capacitive components, which can pose challenges for implementation as a BIST or online testing method.

In this paper, we introduce a structural defect-oriented test for analog and mixed signal circuits, solely utilizing digital monitoring circuits. This approach achieves 100% of defect coverage without altering the circuits topology and incurs with minimum area overhead. In this approach, we first identify the critical nodes of the circuit, and then we develop a test mechanism using external injector circuitry or by operating the circuit itself in a specific test mode. Finally, using the digital monitors, the occurrence of the defects is detected by change in the digital output of monitors from defect-free code to faulty code. The proposed test method can be employed as a post manufacturing test or as an in-field structural test targeting the latent defects. The proposed method is demonstrated on the successive approximation (SAR) analog-to-digital converter (ADC), as a case study. We performed a full structural test on 12-bit ADC designed in 65nm technology node.

The rest of the paper is organized as follows. In Section II, the approach to the digital-like built-in structural test for AMS circuits is discussed. In Section III, we discuss the defect universe and simulation method for high-speed defect coverage test. We demonstrate the proposed structural test for SAR ADC in Section IV. Section V will include the simulation results of the defect-oriented BIST for SAR ADC based on the proposed method. Finally, Section VI, concludes the paper.

II. DIGITAL-LIKE DEFECT ORIENTED TEST

As mentioned earlier, developing a defect-oriented BIST for AMS circuits is a challenging task. Part of the challenge lies in adhering to the general principals of developing BIST for any type of circuits, regardless of its domain of operation. The main requirements in designing of BIST is its transparency with respect to the main circuit. BIST should have zero effect on the normal operation of the circuit. In addition to this, BIST should be fast and have small area and power overhead in comparison to the main circuit. For digital circuits, meeting these main BIST requirements is generally easier compared to AMS circuits, primarily due to the significantly higher sensitivity of AMS circuits. Moreover, the occurrence of a defect has a more noticeable effect on a digital circuit. Most of the hard defects in digital circuits would be manifested by a stuck-on high or stuck-on low logic, which can be detected with near zero additional resources. However, in AMS circuits, a similar defect might not significantly change the performance of the circuit.

We propose a defect-oriented BIST for AMS circuits that exclusively utilizes digital circuits, resulting in lower power consumption and typically smaller area requirements compared to AMS circuits. Additionally, digital-like AMS BIST can itself be tested using digital methods before performing the test on the AMS circuits. Furthermore, the digital-like AMS BIST is also easier to migrate from one technology node to another, reducing the need for redesign of BIST. Using digital-like BIST, the result of the test can be easily routed for inference within IC using well-defined digital protocols.

Figure 1 depicts the main concept for the procedure of designing a Digital-like BIST for AMS circuits. First the AMS circuit needs to be divided into smaller subcircuits of the analog or mixed-signal circuits, such as operational amplifiers, comparators, filters, switches, etc. These circuits should then be analyzed to identify their crucial defect-sensitive nodes. These nodes are the connection points whose values can significantly deviate from the nominal values in the event of a defect. PVT and mismatches must be carefully considered when selecting these nodes and recording their respective value. If PVT and mismatches are not correctly accounted for, a false defect flag might rise even when the circuit is defect-free.
The next step is to put the circuit into a test mode operation so that, by monitoring the selected nodes, the occurrence of a defect can be distinguished from normal operation. Ideally, at this stage, the circuit under the test should be put in the test mode without adding any extra BIST circuitry. However, if the BIST circuitry or “injector circuit” is required for increasing the defect visibility, they must be minimal in size. More importantly these injector circuits must have negligible effect on the normal operation of the circuit under the test.

Finally, a comprehensive simulation must be performed to ensure the target defect coverage is achieved. During the simulation, all the defects defined in the defect universe must be simulated, considering PVT and mismatches. This extensive simulation is required to validate the correctness and robustness of the developed test method. The defect simulation method that we primarily introduced in [12]–[14], reduces simulation time tremendously, cutting simulation time from a few days to couple of hours. In the following sections, we discuss the defect simulation method further.

Lastly, if based on the simulation results, the target defect coverage is achieved, the BIST defect-oriented method for the circuit is developed. Otherwise, the injectors or the test operation mode must be revised so that the defect coverage is improved.

We demonstrated the defect-oriented BIST for an operational amplifier (OA) in our earlier work, presented at ITC’20 [15]. In this work, since the circuit is already quite simple, there is no need to break the circuit into smaller subcircuits. We use the intentional offset injection circuitry as an injector circuit for OA defect-oriented BIST [15], [16]. Digital window comparators, which are simply a combination of different inverters with specifically designed transition threshold voltages, are used as monitors for detecting the defects.

Figure 2 presents the process for the defect-oriented BIST for SAR ADC based on the proposed concept, which we introduced an earlier version here [17]. The circuit is first divided into three smaller subcircuits: comparator, capacitive DAC and binary switches, and sampling switch. Crucial nodes for each of these three subcircuits are then identified, e.g., input of comparator, or top plate of binary capacitive array. For SAR ADC, there is no need for any external injector circuits. Using the operation of the circuit itself a test mode is developed for each of the three subcircuits that will be discussed in depth in the later sections. Finally, comprehensive simulations were performed for each of these subcircuits, testing the robustness and correctness of the test methods for each defect. Utilizing the presented approach, results show a 100% defect coverage for SAR ADC.

III. HIGH-SPEED DEFECT SIMULATION AND DEFECT UNIVERSE

The six common defects—open drain, open gate, gate-source short, gate-source short, and drain-source short—are considered for defect coverage in this work. For fast and accurate simulation, the models in Figure 3 are used which are in accordance with P2427 Standard draft [18]. In these models that we introduced primarily here [13], defects are realized by using a specific placement of resistors. The value of these resistors’ change based on the defect that is being tested.

Table I summarizes the values for these resistors for inducing each of the six defects. For example, $R_{\text{nm}, \text{short}}$ is a resistor that should be realized as a shorted circuit in a defect-free scenario and therefore has a value of 0 $\Omega$ in this case. Similarly, in a defect-free situation, $R_{\text{nm}, \text{open}}$ is realized as an open circuit and ideally must be $\infty$ $\Omega$ (Modeled using 0A current source). $R_{\text{nm, short}}$ acts as a shorted circuit in the case of a short defect and, depending on the defect model, can take a value in the range of 1$\Omega$ to 100 $\Omega$. $R_{\text{nm, open}}$ emulates an open circuit in the case of a

<table>
<thead>
<tr>
<th>Defect</th>
<th>$R_{\text{DD}}$</th>
<th>$R_{\text{SS}}$</th>
<th>$R_{\text{SG}}$</th>
<th>$R_{\text{GD}}$</th>
<th>$R_{\text{DS}}$</th>
<th>$R_{\text{GD}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open Source</td>
<td>$R_{\text{nm, short}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
</tr>
<tr>
<td>Gate Open</td>
<td>$R_{\text{nm, short}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
</tr>
<tr>
<td>Gate short</td>
<td>$R_{\text{nm, short}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
</tr>
<tr>
<td>Drain short</td>
<td>$R_{\text{nm, short}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
</tr>
<tr>
<td>GS short</td>
<td>$R_{\text{nm, short}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
<td>$R_{\text{nm, open}}$</td>
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defect and, depending on the defect model, can have any value greater than 1MΩ.

For instance, when modeling the drain-open defect, all the resistors in the model—\( R_{SS}, R_{GG}, R_{GD}, R_{GS}, R_{DS}, \) and \( R_{GGG} \)—take values identical to the defect-free model. \( R_{DD} \), however, takes the value of the open circuit resistor, \( R_{th,open} \), which is defined as a parametric attribute.

The resistors \( R_{DD}, R_{SS}, R_{GG}, R_{GD}, R_{GS}, R_{DS}, \) and \( R_{GGG} \) are modeled in Verilog-A. Two new terminals named \( V_C \) and \( V_G \) are defined for them. Based on the model defined, the values of these resistors are evaluated by defining an equation in the model that includes the value of \( (V_C - V_G) \), the id of the transistor (referred to as \( \text{fet}_id \)) and the number of defect—0 for defect free to 6—that is required to be tested. With \( V_G \) grounded in the design and allocating different \( \text{fet}_id \) value to each transistor in the circuit under the test (CUT), we only need to assign an appropriate value for \( V_C \) to emulate a specific defect for a specific transistor in the design. Using this model, any defect can be tested in a very short time without changing the configuration of the design for testing each defect. The introduced model also enables consecutive simulations for numerous defect scenarios, which remarkably reduces the simulation time.

IV. SAR ADC: A CASE STUDY

A. Structure of SAR ADC

A 12-bit SAR ADC in 65nm technology was designed for the demonstration and testing of the proposed digital-like defect-oriented BIST. Figure 4 depicts the general structure of the SAR ADC, which includes the binary weighted capacitive DAC, a comparator, and a successive approximation register (SAR) control. The capacitive DAC is a segmented structure with two segmented 6-bit binary weighted capacitive segments for area efficiency. The bottom plate of the capacitive array in the DAC is either connected to the ground line through an NMOS switch, or to the VDD line through a PMOS or to Vin—sampling signal—through the sampling switch, as presented in Figure 4.

The sampling switch used in this work is an enhanced constant \( V_{GS} \) bootstrapped switch depicted in Figure 6. The main advantage of this conventional sampling switch is its relatively constant Ron with respect to the Vin. Having a relatively constant Ron is enabled by keeping the \( V_{GS} \) of the main switch M1, always equal to VDD, independent of Vin [19].

The comparator for this design is a two-stage comparator including a preamplifier stage and the dynamic latch stage [20]. Figure 5 depicts the schematic view of the comparator, including the preamplifier stage (Figure 5.a), which is a 5-transistor amplifier, and the dynamic latch comparator (Figure 5b) as the second stage. Using the design method introduced in [20], the comparator is designed to have output resolution for input difference of half LSB at a maximum clock speed of 10MHz.

The logic for the ADC can be implemented using series of D-flip flops, thus realized completely in digital domain. Since the domain of the logic control is purely digital, advanced digital methods can be used for performing defect detection for this part. Therefore, for any of the proposed BIST, it is assumed that the logic control has already been tested and operates as expected.

B. Defect-Oriented BIST for SAR ADC

As mentioned earlier, any complex AMS circuit needs to be broken down into smaller subcircuits. As depicted in Figure 2, we breakdown the SAR ADC into comparator, capacitive DAC, and sampling switch. For each subcircuit, we then develop a test based on the analyzed crucial nodes. For the rest of this section, we discuss the test mode developed for each subcircuit in detail.
I. BIST for Comparator

The comparator is a two-stage design, including the preamplifier for achieving the required gain, followed by a dynamic latch to speed up the settling time of the output of the comparator Figure 5. Considering the six defects for CMOS transistors, the total number of the defects in the defect universe for the comparator equals to 102 defects.

By analyzing the operation of the comparator and monitoring the voltages at its different nodes, we developed a test operation mode that promises full defect coverage which requires neither injector circuits for excitation, nor any monitoring circuits.

As depicted in Figure 5, the comparator’s positive input is grounded, and the negative input is connected to the top plate of the capacitive array. So, if we want to have a test mode operation without altering the circuit in any way, the only nodes to which we have relative access are positive input of the comparator (IN_N) and outputs of the comparator. Moreover, we can assign different specific values to IN_N, using the capacitive DAC.

Setting the negative input of comparator to take +LSB voltage level and -LSB voltage level, we notice that we can detect the defects by monitoring the outputs of the comparator, OUT+ and OUT-. If the negative input of the comparator has a voltage level of +LSB, the difference between positive input, \( \text{IN}_P \) and \( \text{IN}_N \) would be -LSB, causing the OUT+ to be at logic low and OUT- to be at logic high level. On the other hand, by having \( \text{IN}_N = \text{LSB} \), the difference of the positive input and negative input will be +LSB, hence OUT+ must be at logic low and, respectively, OUT- must be at logic high.

The output of the comparator takes these logic levels in the mentioned scenarios, if and only if there are no defects in any of the 17 CMOS transistor. However, if any of the mentioned 102 defects occurs—except for drain-source short in M7, that will be discussed in section V—at least one of the two outputs of the comparator changes from the expected logic level to the opposite logic level, in at least one of the +LSB or -LSB scenarios.

Bringing the voltage level at \( \text{IN}_N \) to +LSB is simply enabled by sampling the VDD voltage, meaning setting the Vin to be equal to VDD. Then, connecting the bottom plate of all the bits in the capacitive array to the VDD line, except for the LSB bit, which should be connected to GND. This would be equivalent to setting the code for the DAC to all ‘1’s, except for the LSB bit (111…10).

Similarly, to bring the \( \text{IN}_N \) voltage level to -LSB V, we only need to sample GND level, \( \text{Vin}=0 \), and set the code in DAC to all ‘0’s, except for the LSB bit, which should be set to high logic (000..1).

The presented test mode operation, which only utilizes the ADC resources and requires no additional test circuitry, has been shown to achieve 100% defect coverage. We will discuss the coverage results in depth in the next section.

II. BIST for Capacitive DAC

The BIST for the capacitive DAC is developed by carefully analyzing charge conservation in the capacitive binary array. We introduce the “one-hot” test, which is developed by methodically investigating the effect of each defect on the charging phase and conversion phase, the “one-hot” test consists of two phases: pre-charge and conversion. This test can be performed for any bit and enables full defect detection and diagnosis of the capacitive DAC.

We will explain the introduced “one-hot” test for a random bit called the Kth bit. In the pre-charge phase, all the capacitor arrays will be connected to the GND line through the NMOS switches, except for the \( K_{th} \) bit. The \( K_{th} \) bit will be connected to the VDD line via the PMOS switch, referring to the test name “one-hot.” For the conversion stage, the \( K_{th} \) bit is connected to the GND line during the conversion phase, and a normal binary search will be started from the MSB. Normally, with no defect in the circuit, the expected code after conversion must be all zeros from the MSB to and including the \( k_{th} \) bit and all ones from the \((k-1)_{th}\) bit to the LSB. However, the occurrence of a defect can change this code enabling us to detect the defect.

By analyzing the conversion equations for the defect-free and defective cases, we can observe how each defect will affect the expected code. In the defect-free case, based on the charge conservation law, we can write the following equation as the total charge stored after the pre-charge stage:

\[
Q_T = V_{\text{ref}} \cdot 2^k \cdot C_{\text{unit}}
\]

Starting from the above equation and writing the equations for each conversion step, the effect of any defect in the PMOS and NMOS switches of the \( K_{th} \) bit and any bit more significant than the \( k_{th} \) bit can be identified in the converted code.

Let us takes any open defect of the kth bit’s PMOS switch as an example. In this case, the total charge stored in pre-charge stage will be zero, and the converted code received after the test will be the defect-reflected code of all zeros. Now, let us consider any open defect for an NMOS switch at the “\( j_{th} \)” bit \((j>k)\) as another example. In this case, the total charge stored from the pre-charge stage will be as follows:

\[
Q_T = V_{\text{ref}} \cdot 2^k \cdot C_{\text{unit}} + V_j \cdot 2^j \cdot C_{\text{unit}}
\]

In the above equation, \( V_j \) represents the potential stored in the \( j_{th} \) bit’s capacitor, which is unknown. If we perform the normal binary search from the MSB, three situations can be considered:

1) Conversion for bit \( i \) and \( i > j > k \):

By writing the conservation equations and deriving them to determine the voltage value at the negative input of the comparator, \( V_N \), we will have the following equation:

\[
V_{\text{ref}} \left( \frac{2^k \cdot C_{\text{unit}}}{C_{\text{Total}} - 2^k \cdot C_{\text{unit}}} - \frac{2^k \cdot C_{\text{unit}}}{C_{\text{Total}} - 2^k \cdot C_{\text{unit}}} \right) = V_N
\]

\( C_{\text{Total}} \) is the summation of the weights of the capacitors in the capacitive DAC, and \( 2^k \cdot C_{\text{unit}} \) is the weight of the capacitor at the \( k_{th} \) bit. Similarly, \( 2^k \cdot C_{\text{unit}} \) will be the weight of the capacitor array at the \( i_{th} \) bit. Since \( i > k \), the value of \( V_N \) derived from equation (3) will be positive, and the comparator’s output will be ‘0’, not reflecting the defect.
2) Conversion for bit \( j \):

Now when writing the conversion equation for bit \( j \), value of \( V_N \) for this step will be:

\[
V_{\text{ref}} \left( \frac{\sum_{k \neq j} C_{\text{unit}}}{C_{\text{Total}}} - \frac{2^k C_{\text{unit}}}{C_{\text{Total}}} \right) - V_j \left( \frac{\sum_{k \neq j} C_{\text{unit}}}{C_{\text{Total}}} \right) = V_N \quad (4)
\]

The term including \( V_{\text{ref}} \) on the left side of the equation is positive since \( j \neq k \). However, the total value of the left-hand side of equation (4) depends on the value of \( V_j \). Although we do not know \( V_j \), we know that it cannot take a negative value. So, considering the worst case—from a defect detection point of view—\( V_j \) will be ‘0’, and \( V_N \) will be positive, leading to a ‘0’ for the comparator’s output and no reflection of the defect in the code.

3) Conversion for bit \( i \) and \( i \neq j \):

For this step of conversion, the equation for determining \( V_N \) is as follows:

\[
V_{\text{ref}} \left( \frac{2^j C_{\text{unit}}}{C_{\text{Total}}} - \frac{2^k C_{\text{unit}}}{C_{\text{Total}}} \right) + (V_{\text{ref}} - V_j) \left( \frac{\sum_{k \neq j} C_{\text{unit}}}{C_{\text{Total}}} \right) = V_N (1 - \frac{2^k C_{\text{unit}}}{C_{\text{Total}}} ) \quad (5)
\]

The \( (1 - 2^k C_{\text{unit}}/C_{\text{Total}}) \) term on the right-hand side is positive, hence not changing the sign of the left side of the equation when dividing the left side by this term. The second term on the left side of the equation is also positive since \( V_{\text{ref}} \) is always greater than \( V_j \). However, to determine the sign of the first term, we need to consider the value of ‘i’ in comparison with ‘k’.

1) If \( i \neq k \): the first term only, including \( V_{\text{ref}} \), will be negative. In this case \( V_N \) can be positive or negative depending on \( V_j \), and the \( i \text{th} \) bit in converted code can be ‘0’ or ‘1’.

2) If \( i \neq k \): the first term will be positive, resulting in a positive value for \( V_N \) and a ‘0’ at the comparator’s output. Since \( i \neq k \), the defect-free code for this bit should be ‘1’, but now we are receiving a ‘0’ for this bit thus detecting the defect.

If we analyze the conversion steps in the presence of each defect for all the bits, we notice that the defects can be detected as an alteration in the expected defect-free code.

III. BIST for constant \( V_{GS} \) bootstrapped Switch

The bootstrapped switch shown in Figure 6 is the commonly used switch for connecting the \( V_{\text{in}} \) line to the capacitor array. The switch consists of 10 CMOS transistors. Considering the mentioned six defects defined for CMOS transistors and two short and open defects for the bootstrapped capacitor, \( C_{\text{bs}} \), the total defects possible for the defect coverage consideration adds up to sixty-two.

With comprehensive nodal analysis of the bootstrapped switch, in the presence and absence of each defect, we can identify the crucial nodes as \( V_{\text{out}} \), \( V_{G1} \), and \( V_{G8} \). We can take the gate-drain short defect in transistor M11, as an example, illustrating the detection of the defect through monitoring the node \( V_{\text{out}} \). If we set \( V_{\text{in}} \) to be equal to \( V_{\text{DD}} \), the voltage at \( \text{Vout} \) node should also be at the \( V_{\text{DD}} \) level while the \( \text{CLK} \) is high. When \( \text{CLK} \) is low, it must remain at logic high since \( M1 \) is off. However, if a gate-drain short occurs in \( M1 \), the \( V_{\text{out}} \) voltage drops to \( \text{GND} \) level through \( M9 \) and \( M10 \) transistors.

By employing three digital detectors to monitor the crucial voltage nodes \( V_{\text{out}} \), \( V_{G1} \), and \( V_{G8} \), all 62 possible defects are detected achieving a 100% detect coverage. These detectors are shown in Fig. 6, distinguished from the main circuit by blue color.

The monitoring detectors used are simple inverters specifically designed to monitor the respective nodes. The design of the monitors starts with categorizing the defects based on the node that can identify them. Then, we record the out of the range voltages gathered by conducting comprehensive PVT and Monte Carlo (MC) simulations for each defect in each category. Finally, based on the collected data, detectors are designed to identify their designated defects under and voltage, temperature, or process variation.

IV. SIMULATION RESULTS

Comprehensive simulations were performed for each of the test methods proposed in previous section to ensure the correctness and robustness of the proposed BIST. Simulations were conducted while considering the fact that the probability of multiple defects occurring simultaneously is very low [21]. Therefore, for each defect simulation, only one defect was induced at a time, and its effect was investigated. Defect coverage for this work is calculated based on the universal defect coverage equation as follow [4]:

\[
\text{Defect Coverage} = \frac{\text{Weighted total number of defects detected}}{\text{All defects in circuit's defect Universe}} \times 100 \quad (6)
\]

The numerator of the defect coverage equation is generally defined as the weighted number of the total defect to account for the different probability of the defect occurrences [22]. However, in most cases the probability of occurrence is considered equal for all defects. In this work, assuming that defects have the same probability of occurrence or different probabilities does not affect the defect coverage, as all defects are detected.

A. Comparator

Table II lists the expected outputs of the comparator with different induced voltage levels given to \( \text{IN}_N \) of the comparator. Before conducting any defect coverage simulation, we ensured that the values of the output remain as expected, considering PVT and mismatches. Figure 7 shows the MC simulation results for the comparator’s output, \( \text{OUT}+ \) with +\( \text{LSB} \) for \( \text{IN}_N \).

<table>
<thead>
<tr>
<th>( \text{IN}_N ) (V)</th>
<th>( \text{OUT}+ )</th>
<th>( \text{OUT}- )</th>
</tr>
</thead>
<tbody>
<tr>
<td>+( \text{LSB} )</td>
<td>‘0’</td>
<td>‘1’</td>
</tr>
<tr>
<td>-( \text{LSB} )</td>
<td>‘1’</td>
<td>‘0’</td>
</tr>
</tbody>
</table>

Table II: Truth table for comparator BIST
Each defect for each transistor was then induced one at a time and different PVT cases were simulated. Moreover, for each defect, 200 MC simulations were conducted [23], validating the BIST with respect to local and global variation and mismatches. As an example, Figure 8 depicts the histogram for 200 MC simulation in the presence of a gate-open defect in transistor M6. In a defect-free scenario, with a +LSB voltage at IN_N, we expect a logic high, or near VDD value, at OUT+. However, in the Figure 8, we can observe that the voltage at OUT+ for all the 200 cases is less than 2μV at OUT+, detecting the defect for all the cases.

From the simulation results, it is clear that all defects in the transistors of the preamplifier and the dynamic latch can be detected, except for the drain-source short defect in M7, open-source in M14, and open-gate defect in M15. However, the latter two defects can be easily detected if the input of the comparator is swapped, and the test mode operation defined in the previous section is performed. Since most comparators used in data converters conventionally employ the chopping technique [24–26] to manage input offset, there is no need to implement input swapping circuitry for BIST. Therefore, these two defects can also be considered detectable.

The drain-source short defect in the tail transistor M7 does not affect the performance of the comparator. This defect primarily impacts the amount of leakage current passing through transistor M7. In the dynamic latch circuit, which includes six PMOS transistors, the drain-source short defect in M7 only results in a slight increase in leakage current on the order of parts per million (ppm). Since the quiescent current of the comparator typically falls within the range of hundreds of microamperes (μA) or even milliamperes (mA), the increase in leakage current from a few picamperes (pA) to hundreds of picamperes (pA) does not significantly impact power consumption. This variation in power consumption is relatively small and can be considered negligible when compared to power consumption variations related to PVT effects.

For defect coverage calculation in this case, since the mentioned drain-source short in M7 does not affect the performance of the circuit or endanger its operation, it can be excluded from the defect universe. Therefore, without any added circuitry for the comparator, we have achieved 100% defect coverage.

**B. Bootstrapped Switch**

As mentioned earlier, the digital detectors must be designed considering the PVT and mismatches. Therefore, each defect that is expected to be detected by a detector, is induced into the circuit one at a time. Then, PVT and MC simulations are conducted, and voltage at the crucial node connected to the detector is gathered. Finally, the detector is designed using this data. Table III tabulates the possible defects for each CMOS transistor and summarizes which detector can detect them. As shown in Figure 6 the digital detector designed for the nodes

<table>
<thead>
<tr>
<th>FAULT</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>M7</th>
<th>M8</th>
<th>M9</th>
<th>M10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Open</td>
<td>Vout (1μV)</td>
<td>Vout (1.73V)</td>
<td>VG1</td>
<td>Vout (761μV)</td>
<td>VG8</td>
<td>VG1</td>
<td>VG1</td>
<td>Vout (588μV)</td>
<td>VG8</td>
<td>VG8</td>
</tr>
<tr>
<td>Source Open</td>
<td>Vout (1.31V)</td>
<td>Vout (1.73V)</td>
<td>VG1</td>
<td>Vout (690μV)</td>
<td>VG8</td>
<td>VG1</td>
<td>VG1</td>
<td>Vout (642μV)</td>
<td>VG8</td>
<td>VG8</td>
</tr>
<tr>
<td>Gate Open</td>
<td>Vout (65μV)</td>
<td>Vout (1.73V)</td>
<td>VG1</td>
<td>Vout (588μV)</td>
<td>VG8</td>
<td>VG1</td>
<td>VG1</td>
<td>Vout (588μV)</td>
<td>VG8</td>
<td>VG8</td>
</tr>
<tr>
<td>GD short</td>
<td>VG1</td>
<td>Vout (1.94V)</td>
<td>Vout (1.62V)</td>
<td>VG8</td>
<td>Vout (1.48V)</td>
<td>VG1</td>
<td>Vout (1.40V)</td>
<td>VG8</td>
<td>VG8</td>
<td></td>
</tr>
<tr>
<td>GS short</td>
<td>Vout (1.94V)</td>
<td>Vout (1.47V)</td>
<td>Vout (1.76V)</td>
<td>VG8</td>
<td>Vout (1.47V)</td>
<td>Vout (1.94V)</td>
<td>Vout (666μV)</td>
<td>VG8</td>
<td>Vout (907μV)</td>
<td></td>
</tr>
<tr>
<td>DS short</td>
<td>VG1</td>
<td>Vout (148μV)</td>
<td>Vout (1.76V)</td>
<td>VG8</td>
<td>VG8</td>
<td>VG8</td>
<td>Vout (1.91V)</td>
<td>VG1</td>
<td>VG1</td>
<td>Vout (8μV)</td>
</tr>
</tbody>
</table>
Vout, VG1, and VG8 are Vout_INV, VG1_INV and VG8_INV respectively.

Defect detection is initiated by setting Vin to either VDD or GND level. For instance, defect detection through Vout_INV is enabled when Vin is at the VDD level. With no defect, voltage at Vout should also be near the VDD level. Any defect that makes the voltage of this node less than VDD is detectable by monitoring this node. The worst-case values—highest voltage— for the node Vout, which were gathered from the PVT and MC simulations, are indicated in Table III. For instance, the highest value that the Vout node can take when there is a drain open in M1 is only 1uV and the highest voltage at Vout with having a gate-drain short in M6 is 1.48V.

Now, from this data, we can see that the highest voltage that this node can take and still be monitored by Vout_INV as a defect is 1.94V. Based on this information, the Vout_INV must be designed to have a switching threshold voltage of 1.95V. Ensuring this switching point can be easily done by adjusting the size of the inverter.

Monitoring nodes through VG1 and VG8 is done by setting Vin to be near GND level. The VG1 node takes a VDD value when CLK is high and ‘0’ when CLK is low, anything other than these will be categorized as defect. Similarly, for VG8, with a CLK high, it is near VDD level, and when CLK is low it is near GND level. By performing the PVT and MC simulations for these nodes with their respective designated defects, the target switching threshold of VG1_INV and VG8_INV can be determined. Based on these simulations and considering the worst cases for achieving a full defect coverage, VG1_INV and VG8_INV should have switching threshold voltages of 2.1V and 1.25V respectively.

Figure 9 Shows the characteristic curve of the three detectors for 200 MC simulations each. From the information in the figure, it is certain that even with process variation, the target switching threshold designed for full coverage is achieved. After ensuring the design of the detectors, their performance is validated in the presence of each defect. To cover all situations, simulations for each of the 62 defects are performed considering process and voltage variation (PVT) and 200 cases of MC. An example of the MC simulations for defects is provided in Figure 10, focusing on the gate-drain short in M1. As we mentioned before, with no defect, we expect VG1 to be near VDD level, and VG1_INV to have a logic low as output. In Fig. 9 all the Monte Carlo cases have voltage level output of near 2.5V or logic high for VG1_INV, indicating defect detection for all MC cases of the short defect in M1. The proposed method is robust, detecting defects across PVT and MC with a 100% defect coverage.

C. Capacitive DAC

As discussed in the previous section, with a one-hot test for a bit, we can detect defects in the bit under test and bits more significant than the bit under test. Considering the structure in Fig. 5 with only two one-hot tests for the LSB bit of each section, we can achieve 100% defect coverage and 50% defect localization to the bit level.

However, including the soft defects, the two “one-hot” tests will not be enough for full defect coverage. The soft defects in this circuit refer to deviations in the values of the capacitors, and they may occur in a unit-sized switch of a bit instead of assuming defect occurrence in the whole switch of the bit. In this case, to achieve full coverage, a “one-hot” test must be performed for each bit. This ensures full coverage of all the hard defects as well as the soft defects. Additionally, performing the
test for each bit not only provides full coverage but also increases defect localization to the bit level.

Table IV summarizes the defective code and defect-free code for each defect in the NMOS and PMOS switches for bit 12. We know that the defect-free code when performing a “one-hot” test for bit 12 is ‘0’ at bit 12 and all ‘1’s from bit 11 to the LSB. However, we can see in Table IV that with a drain open defect in a unit-sized PMOS switch of bit 12—a soft defect—the converted code has ‘0’ in several bits instead of ‘1’, hence detecting the defect. Besides, with the bit-level localization enabled by the introduced BIST, we can also achieve a defect diagnosis rate of 82%. This defect diagnosis will provide valuable information for future designs as well as the implementation of functional safety measures for the circuit.

IV. CONCLUSION

In this paper, we introduced a novel approach to address the growing need for defect-oriented testing in AMS circuits. This approach relies on breaking down complex AMS circuits into smaller, more manageable subcircuits, which are then thoroughly tested using purely digital monitors and/or injectors. An important feature of this methodology is its resource-efficient design. Before incorporating any injector or monitoring circuits, careful consideration optimizes the utilization of the circuit’s existing resources. This strategic approach ensures that the proposed BIST minimizes area overhead and power consumption, making it a highly practical and cost-effective solution. The effectiveness of this approach is demonstrated through the development of a BIST for a 12-bit SAR ADC. Importantly, this BIST methodology achieves full defect coverage without additional BIST circuitry for the subcircuits, except for small digital monitors used in the sampling switch BIST. The proposed test mode operation can be seamlessly integrated into the manufacturing process as a post-manufacturing test or employed in the field, running before circuit start-up or at any time on-demand. This flexibility enhances its utility across various applications and industries.

REFERENCES


