A hybrid amplifier topology for low-noise direct-coupled front ends

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Abstract

Hybrid amplifiers combine discrete transistors with operational amplifiers (OAs) achieving superior characteristics compared with commercially available OAs, while keeping simple structures and a reduced number of parts. A single-ended amplifier topology based on a junction field-effect transistor (JFET) is proposed as a means of achieving very low input noise levels, both in current and voltage. It is direct-coupled and allows to place a high-pass filter at its input to preserve input range, or at its output to optimize noise. The proposed topology results in a low input capacitance and low input-current noise, making it suitable for applications where multiple amplifiers are connected in parallel to achieve ultra-low noise levels. The amplifier’s gain is set by a resistor ratio, being suitable for instrumentation front ends. The circuit analysis and design equations are provided to adapt it for different applications and, as an example, an amplifier with a gain of 40 dB and a bandwidth from DC to 1 MHz was designed, built, and tested.
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Abstract—Hybrid amplifiers combine discrete transistors with operational amplifiers (OAs) achieving superior characteristics compared with commercially available OAs, while keeping simple structures and a reduced number of parts. A single-ended amplifier topology based on a junction field-effect transistor (JFET) is proposed as a means of achieving very low input noise levels, both in current and voltage. It is direct-coupled and allows to place a high-pass filter at its input to preserve input range, or at its output to optimize noise. The proposed topology results in a low input capacitance and low input-current noise, making it suitable for applications where multiple amplifiers are connected in parallel to achieve ultra-low noise levels. The amplifier’s gain is set by a resistor ratio, being suitable for instrumentation front ends. The circuit analysis and design equations are provided to adapt it for different applications and, as an example, an amplifier with a gain of 40 dB and a bandwidth from DC to 1 MHz was designed, built, and tested. The dominant noise contribution of the amplifier was the JFET (a JFE2140 device), featuring an input noise voltage of 0.95 nV/√Hz @1 kHz, that is reduced to 0.70 nV/√Hz @1 kHz when two amplifiers are connected in parallel.

Index Terms—Hybrid amplifiers, low-noise amplifiers, JFET input amplifiers.

I. INTRODUCTION

Hybrid topologies composed of discrete Junction Field Transistors (JFETs) and Operational Amplifiers (OAs) provide a simple way to implement front ends featuring both low voltage noise and low current noise, and which are able to work properly with a wide range of signal source impedances [1, 2, 3, 4, 5]. The key to this approach is that the JFET provides a low-noise front end with a gain of typically 20-30 times, thus relaxing the noise requirements for the next stage and allowing its implementation with OAs. There are discrete JFET devices available with voltage noise spectral densities \( \epsilon_{\text{V, JFET}} \) around 1 nV/√Hz and below. This noise density is comparable to that of their Bipolar Junction Transistor (BJT) counterparts but presenting several orders of magnitude lower current noise spectral densities \( \epsilon_{\text{I, JFET}} \) and much higher input impedances \( Z_{\text{in}} \).

Figure 1 shows typical hybrid amplifier topologies that consist in a JFET common-source stage followed by an ac-coupled OA-based amplifier. In the scheme depicted in Fig.1 (a) the two stages are independent [3, 2]. The overall gain \( G_n \) depends on the JFET transconductance \( g_m \) and is therefore not suitable for those applications where a stable and accurate gain is required. This can be solved by a short-term off-line calibration [3] or by an additional fixed-gain channel for on-line calibration [2] but at the expense of introducing a manual start-up procedure or increasing circuit complexity. The noise of the bias resistor \( R_A \) at the JFET source is decoupled by the capacitor \( C_A \) and the overall noise is almost exclusively due to the JFET voltage noise \( \epsilon_{\text{V, JFET}} \). It is important to note that if very low working frequencies are required, the capacitor \( C_A \) becomes very large, up to a few farads [2]. On the other hand, the circuit in Fig.1 (b) does not require large capacitors and includes a feedback path through resistors \( R_p, R_B \) that ensures an accurate gain \( G_n = 1 + R_B/R_A \), but the noise of the source resistor \( R_A \) can not be decoupled and contributes to the overall noise [5, 6, 3, 1].

Both circuits in Fig.1 correspond to ac-coupled amplifiers and their low cutoff frequency \( f_c \) must be designed according to specific needs. A direct-coupled amplifier with a broad bandwidth is a more flexible alternative, since it allows the inclusion of a high-pass filter with \( f_c \) values as close to dc as desired, and this filter can be placed at the input to preserve the input voltage range, or at the output to optimize noise. In addition, the low-impedance output the amplifier provides relaxes the impedance conditions for a subsequent high-pass filter, thus allowing to implement extremely low cutoff frequencies without degrading the noise characteristics. Figure 2 shows two schemes for direct-coupling hybrid amplifiers. The circuit in Fig.2 (a), proposed in [7], is a single-ended amplifier based on a differential pair. It verifies a fixed and accurate gain

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$G_n = 1 + R_B/R_A$, the noise contribution of $R_A$ can be made negligible selecting a low value resistor [5, 1] but both JFETs contribute to the overall noise that results in almost $\sqrt{2}$ times $e_{\text{FET}}$ [2]. An input-referred noise $e_{\text{in}}$ very close to $e_{\text{FET}}$ can be achieved with the direct-coupled circuit proposed in [4] that does not include a bias resistor at the source node of the JFET ($I_b = I_DSS$). It also ensures a fixed drain voltage $V_D$ thus reducing the Miller effect [8] and, consequently, the input capacitance $C_{in}$, but its gain $G_n$ depends on the JFET transconductance $g_m$. The circuit herein proposed solve this issue by adding a feedback path that ensures a fixed gain $G_n$ while preserving the condition for a low $C_{in}$ and allowing to set a drain current below $I_DSS$. The main characteristics of the mentioned topologies are summarized in Table 1.

The term $e_{\text{FET}}$ refers to the noise contribution of the resistor connected at JFET source terminal which is necessary for setting the amplifier gain. It can be made negligible selecting a low-enough resistor value.

### II. PROPOSED TOPOLOGY

The proposed topology, presented in Fig.3, originates from the one depicted in Fig.1 (b); however, the stages are not ac-coupled but direct-coupled: the biasing and signal behavior are no longer independent but interact with each other. The amplifier gain is $G_n = 1 + R_B/R_A$ and the Drain voltage $V_D = V_{b}$ is constant, thus reducing the Miller effect leading to low input capacitances $C_{in}$ [5].

### A. Operating point analysis

The JFET biasing is controlled in a closed loop scheme. Note that the virtual ground at the OA inputs ensures a Drain current $I_D$ given by:

$$I_D = (V_R - V_B)/R_D, \quad (1)$$

where $V_R$, $V_B$ and $R_D$ are the voltage sources and the Drain resistor indicated in Fig.3. The relationship between $I_D$ and the Gate-Source voltage $V_{GS}$ can be approximate by a quadratic function given by:

$$I_D = I_{DSS}(1 - V_{GS}/V_{GSC})^2 \quad (2)$$

where $I_{DSS}$ is the JFET saturation current, $V_{GSC}$ its cutoff voltage and $V_{GS}$ is set by the voltage drop over $R_D$ produced by $I_D$ and the OA output voltage $V_O$ as:

$$V_{GS} = I_D R_{AB} + V_O R_A/(R_A + R_B). \quad (3)$$

Obtaining $V_{GS}$ from (2), replacing it in (3) and using $G_n=(R_A + R_B)/R_A$ leads to:

$$V_O = \left( V_{GSC} \left(1 - \sqrt{I_D/I_{DSS}} \right) - I_D R_{AB} \right) G_n, \quad (4)$$

that must be between the power-supply rail voltages $V_{OMIN}$ and $V_{OMAX}$ verifying:

$$V_{OMIN} < V_{GSC} \left(1 - \sqrt{I_D/I_{DSS}} \right) G_n - I_D R_B < V_{OMAX} \quad (5)$$

Figure 4 shows this constrain for typical parameter values of $V_{GSC}$ and $I_{DSS}$ of the JFE2140 from Texas Instruments [10]. $R_A=10 \, \Omega$ and different $G_n$ settings. As can be observed, higher $G_n$ values result in higher $V_O$ voltages. Nominal gain $G_n$ values of $30-100$ times ($\approx 30-40 \, \text{dB}$) are feasible, which are usual and enough to relax the noise requirements of the subsequent stage.

It is important to note that a DC bias voltage is present at the amplifier’s output. However, since a $30-40 \, \text{dB}$ gain is provided in combination to a low output impedance, there are many techniques available to reject this bias voltage and achieve very low cutoff frequencies without the need for high-value capacitances.

#### Table 1. Comparison of the proposed topology with other works.

<table>
<thead>
<tr>
<th>Input referred voltage noise</th>
<th>Large-value capacitors</th>
<th>Direct coupled</th>
<th>Stable gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>$e_{\text{FET}} + e_{\text{R}}$</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>[7]</td>
<td>$e_{\text{FET}}\sqrt{2} + e_{\text{R}}$</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>[1],[5]</td>
<td>$e_{\text{FET}} + e_{\text{R}}$</td>
<td>NO</td>
<td>NO</td>
</tr>
<tr>
<td>[4]</td>
<td>$e_{\text{FET}}$</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>[3]</td>
<td>$e_{\text{FET}}$</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>[2]</td>
<td>$e_{\text{FET}}$</td>
<td>YES</td>
<td>NO</td>
</tr>
</tbody>
</table>

Table 1. * This amplifier includes an ac coupling network at the input, but simply by removing it, the circuit can work as a direct-coupled amplifier. **This scheme requires an additional channel for gain calibration purposes.

Figure 3. Proposed direct-coupled hybrid topology for low-noise amplifiers.
then referring it to the input, the input-referred overall noise is given by:

\[ e_i^2 = e_{FB}^2 + e_{RA}^2 + \left( \frac{e_{RB}}{G_n} \right)^2 + \left( \frac{i_{nA}}{g_m} \right)^2 + \left( \frac{e_{VR}}{G(s)} \right)^2 + \left( \frac{e_{VB}}{G(s)} \right)^2 + e_{nA}^2 \]

(7)

Considering that even for bipolar OA devices \( i_{nA} \) is of just a few pA/\( \sqrt{\text{Hz}} \) and \( g_m \) values of tens of mS, the term \( i_{nA}/g_m \) results of the order of tenths of nV/\( \sqrt{\text{Hz}} \) can be neglected. The term \( e_{RB}/G_n \) can also neglected against \( e_{RA} \) because \( e_{RB}/G_n \ll e_{RA} \). Finally, the total input-referred noise can be approximated by:

\[ e_i^2 \approx e_{FB}^2 + e_{RA}^2 + \frac{e_{VR}^2 + e_{RB}^2 + e_{VB}^2 + e_{nA}^2}{(g_m R_D)^2} \]

(8)

The above equation is valid for instantaneous values of deterministic signals, but random signals as noise are described by statistical features such as standard deviation in Volts (RMS value) or spectral densities expressed in \( V^2/\text{Hz} \) or \( V/\sqrt{\text{Hz}} \). Assuming that the different noise sources in (6) are statistically independent, the mean square value \( e_i^2 \) of the input-referred noise is given by:

\[ e_i^2 \approx e_{FB}^2 + e_{RA}^2 + \frac{e_{VR}^2 + e_{RB}^2 + e_{VB}^2 + e_{nA}^2}{(g_m R_D)^2} \]

The proposed circuit presents constant transfer functions within the bandwidth of interest. Then, (8) also expresses the noise spectral density with just a change of units from \( V^2 \) to \( [V^2/\text{Hz}] \).

Considering that the JFET voltage noise \( e_{FB} \) is around 1 nV/\( \sqrt{\text{Hz}} \), then the other contributions should be minimized as much as possible compared to this value. The noise of \( R_A \) appears directly at the input, and to ensure \( e_{RA} \approx 1 \) nV/\( \sqrt{\text{Hz}} \) a resistor below 10 \( \Omega \) should be used. As a reference, the contribution of a resistor \( R_A \) of 10 \( \Omega \) that presents a thermal noise \( e_{RA} \approx 0.41 \) nV/\( \sqrt{\text{Hz}} \) increases the overall noise by around 8\%: \( e_i^2 \approx 1^2 + 0.41^2 = 1.08^2 \).

The gain \( g_m R_D \) provided by the JFET stage is around 20-30 times and as can be seen from (8), it relaxes the noise constrains for \( e_{VR}, e_{RB}, e_{VB} \) and \( e_{nA} \). However, their overall noise contribution should be less than 10 nV/\( \sqrt{\text{Hz}} \) to achieve \( e_i \) values close to \( e_{FB} \). In this condition, (8) can be approximate as:

\[ e_i^2 \approx e_{FB}^2 + e_{RA}^2 \]

(9)

C. Frequency response and stability issues

The JFET stage provides a gain of \( g_m R_D \). If unity-gain stable OAs are used, the circuit does not present stability problems when a closed-loop gain \( G_\alpha \) greater than \( g_m R_D \) is set. This is because the attenuator \( \frac{R_A}{(R_A+R_D)} = G_\alpha^{-1} \) reduces the open loop gain more than the JFET increases it. In this condition the amplifier open-loop gain is \( G_{DL}(s) = g_m R_D A(s)/G_n \) and the closed-loop gain \( G(s) \) is given by:

\[ G(s) = \frac{g_m R_D A(s)}{1 + g_m R_D A(s)/G_n}, \]

(10)

where \( A(s) \) is the OA open-loop gain. For low frequencies (10)
verifies \( G(s) \approx G_n \). The amplifier frequency response depends on \( A(s) \) and could present a resonant peak depending on the OA phase margin. A smooth response can be ensured by adding a feedback capacitor \( C_F \) as Fig.6 shows. In this case the OA works as a transimpedance amplifier, the open-loop gain becomes \( G_{ol}(s) = g_m/sC_FG_n \) and the closed-loop gain \( G(s) \) results:

\[
G(s) = \frac{g_m/sC_F}{1 + g_m/sC_FG_n},
\]

which can be rearranged as:

\[
G(s) = \frac{G_n}{1 + sC_FG_n/g_m},
\]

thus verifying a first order response with a low frequency gain \( G_n \) and a -3 dB cutoff frequency \( f_c \) given by:

\[
G_n = 1 + R_B/R_A ; \ f_c = \frac{g_m}{2\pi C_F G_n}.
\]

Then, by including \( C_F \) the amplifier bandwidth is reduced, but its frequency response becomes independent of \( A(s) \).

![Fig. 6. The circuit is stable for closed-loop gains \( G_n > g_m R_B \) but could present a resonant peak depending on the OA open-loop gain \( A(s) \). By including the capacitor \( C_F \), the frequency response of the amplifier becomes independent of \( A(s) \) and verifies a single pole low-pass transfer function.](Image)

III. EXPERIMENTAL RESULTS

In order to validate the proposed topology and its circuit analysis, an amplifier with a gain \( G_n=40 \text{ dB} \) and a bandwidth of 1 MHz was built and tested. A resistor \( R_A=10 \Omega \) was adopted which does not contribute significantly to the overall noise, and a resistor \( R_B=1 \text{ kΩ} \) to set the desired nominal gain \( G_n=40 \text{ dB} \). The amplifier was implemented with the transistor JFE2140 and the low-noise operational amplifier OPA211, both devices from Texas Instruments.

The JFE2140 was biased at \( I_P=11 \text{ mA} \), this is slightly below its minimum \( I_{DSS} \) value which is of 12 mA [10], and \( V_{DS}=3 \text{ V} \). This was achieved according to (1) by setting \( V_R=14 \text{ V}, V_B=3 \text{ V}, \text{ and } R_P=1 \text{ kΩ} \). Finally, the circuit components’ values result: \( V_R=14 \text{ V}, V_B=3 \text{ V}, R_A=10 \Omega, R_B=1 \text{ kΩ} \).

The bias approach leads to \( I_D \) values close to \( I_{DSS} \) to avoid large OA voltages and output currents. If lower \( I_D \) values are desired, devices with lower \( I_{DSS} \) should be used, such as the LSK389A.

As can be observed from (8), the voltage sources \( V_R, V_B \) must present low noise, which is usually solved by using high-capacity batteries as in [4, 5, 9]. To achieve a compact implementation, these voltages were obtained from stacking direct biased diodes, filtering and buffering \( V_R \) with an inexpensive NE5532 as is shown in the Appendix. The circuit was powered by Li-Po 18650 batteries composing a +18V/-12V power supply.

A. Input referred voltage noise

The amplifier input was short-circuited, and its noise voltage spectral density measured by using an Agilent 35670A Signal Analyzer. The measured spectral density (input-referred) is shown in Fig.7 in blue. It is 0.95 nV/√Hz@1 kHz, increasing to 7 nV/√Hz@1 Hz. Then, two amplifiers were connected in parallel through a passive adder composed of two 1 kΩ resistors as in [11], thus providing a 500 Ω impedance output and resulting in the noise spectral density indicated in red in Fig.7. Note that the noise is reduced around \( \sqrt{2} \) times, leading to 0.70 nV/√Hz @1 kHz and 5.0 nV/√Hz @1 Hz.

![Fig. 7. In blue is indicated the input-referred noise spectral density \( e_i \) of the built amplifier, and in red the resulting \( e_i \) connecting two identical amplifiers in parallel. In dashed line is indicated the expected noise of the JFE2140 for \( I_D=5 \text{ mA} \) from its datasheet.](Image)

B. Resistors’ noise measurements

Figure 8 shows the input-referred noise for different source resistors \( R_S \) connected directly at the amplifier’s input. As it can be observed, for \( R_S\geq1 \text{ kΩ} \) the measured noise agrees with that expected for the resistor thermal noise (indicated in dashed lines). For \( R_S=1 \text{ MΩ} \) the cutoff frequency is around 20 kHz, suggesting an input capacitance \( C_{in} \approx 8 \text{ pF} \) that includes the JFET input capacitance and the capacitance associated with printed circuit board traces.

C. Frequency Response

The frequency response of the implemented amplifier was measured using an Agilent DSO-X 2024A oscilloscope and its embedded signal generator resulting in the curve indicated in
blue in Fig. 9. The amplifier gain is 39.9 dB for frequencies up to 1 MHz, remaining inside a ±0.1 dB band, and presents a resonant peak around 5 MHz. Then, a compensation capacitor $C_p = 20 \text{ pF}$ was included as Fig. 6 shows to produce a smoother response resulting in the curves in red. Experimental data are indicated in dots while the simulation results obtained with SPICE software TINA from Texas Instruments are indicated in continuous line. The frequency response for $C_p = 20 \text{ pF}$ considering $g_m = 18 \text{ mS}$ is also shown in Fig. 9; the simulation results for this condition are presented in dotted line as well but resulted in close superposition to the experimental data. In this case the −3 dB bandwidth reduces to 1.2 MHz.

IV. CONCLUSIONS

The proposed topology results in direct-coupled amplifiers with a well-defined gain $G_a$ that does not introduce phase shifts within the signal bandwidth, being thus appropriate to work as a front end and inside closed-loop schemes.

The overall noise is close to that of the JFET in the first stage, and voltage and current noise levels below $1 \text{ nV/} \sqrt{\text{Hz}} @ 1 \text{ kHz}$, $2 \text{ fA/} \sqrt{\text{Hz}} @ 1 \text{ kHz}$ can be easily achieved with medium-grade devices. The JFET provides a gain of around 20 times and relaxes the admissible noise of the subsequent stage, which can therefore be implemented by using an operational amplifier. Moreover, the current input noise of the JFET is very low, thus allowing to connect several ($N$) amplifiers in parallel reducing the overall noise by $\sqrt{N}$ [11]. The feasibility of this approach is bolstered in this work given that the proposed amplifier is very simple, requires a reduced number of parts, and employs low-cost components. A usual practice is to connect several JFETs in parallel to reduce noise [1] by reducing the JFET noise contribution, but other contributions remain and could become dominant for large $N$ values. By connecting independent amplifiers in parallel, all their noise sources contributions are reduced.

Drain current $I_D$ and voltage $V_D$ are set by a closed loop scheme, resulting in a stable and well-defined operation point. This approach also reduces the Miller effect, which leads to low input capacitances. There is a trade-off between the desired $I_D$, the power supply voltage rails, and the amplifier gain $G_a$, but setting $I_D$ close to the device saturation current $I_{DS}$, $G_a$ values up to 30-40 dB are feasible without including trimmings.

The proposed scheme allows for simple frequency response compensation by including a capacitor to limit the bandwidth and ensure a first-order low-pass response. All design equations have been provided and experimentally verified.

V. APPENDIX. AUXILIARY VOLTAGES CIRCUIT

Figure 10 depicts the circuit used in the experimental tests to obtain the voltages $V_A$ and $V_B$. 

Figure 10. Circuit used in the tests to obtain the auxiliary voltages $V_A$ and $V_B$. 

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Fig. 8. Voltage noise spectral density for different $R_1$ resistors connected at the amplifier’s input. The thermal noise corresponding to each resistor value is indicated in dashed line.

![Fig. 8](image1.png)

Fig. 9. Frequency response of the implemented amplifier without the compensation capacitor $C_p$ (in blue) and including it (in red). Experimental results are indicated in dotted line and simulation results in continuous line.

![Fig. 9](image2.png)
VI. References


