Current-Limiting Control of Grid-Forming Inverters: State-of-the-Art and Open Issues

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Abstract

Grid-forming (GFM) inverters are recognized as a viable solution to increase the penetration of renewable energy in bulk power systems. However, GFM inverters are physically different from synchronous generators (SGs) in terms of fault current level. To protect the GFM inverters and support the power grid under faults or severe disturbances, various current-limiting control methods are developed. In this paper, an overview of these methods is presented, which can be classified as direct, indirect, and hybrid ones. An overall control diagram of GFM inverters is developed to demonstrate the implementation of different current-limiting controls. The advantages and disadvantages of different methods are also illustrated. Finally, open issues of current-limiting control methods for GFM inverters, including control stability, fault recovery, and fault current injection, are summarized.
Current-Limiting Control of Grid-Forming Inverters: State-of-the-Art and Open Issues

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Abstract—Grid-forming (GFM) inverters are recognized as a viable solution to increase the penetration of renewable energy in bulk power systems. However, GFM inverters are physically different from synchronous generators (SGs) in terms of fault current level. To protect the GFM inverters and support the power grid under faults or severe disturbances, various current-limiting control methods are developed. In this paper, an overview of these methods is presented, which can be classified as direct, indirect, and hybrid ones. An overall control diagram of GFM inverters is developed to demonstrate the implementation of different current-limiting controls. The advantages and disadvantages of different methods are also illustrated. Finally, open issues of current-limiting control methods for GFM inverters, including control stability, fault recovery, and fault current injection, are summarized.

Index Terms—Grid-forming (GFM) inverter, current-limiting control, control stability, fault recovery, fault current injection.

NOMENCLATURE

\( \theta \) \hspace{1cm} \text{the phase angle generated by the outer loops, in rad}
\( E \) \hspace{1cm} \text{the voltage magnitude generated by the outer loops, in p.u.}
\( I \) \hspace{1cm} \text{the inverter output current magnitude, in p.u.}
\( i \) \hspace{1cm} \text{the inverter output current, in p.u.}
\( I_M \) \hspace{1cm} \text{the maximum allowed current magnitude, in p.u.}
\( i_{ref} \) \hspace{1cm} \text{the saturated output current reference, in p.u.}
\( P \) \hspace{1cm} \text{the inverter output active power, in p.u.}
\( P_{ref} \) \hspace{1cm} \text{the saturated active power reference, in p.u.}
\( Q \) \hspace{1cm} \text{the inverter output reactive power, in p.u.}
\( Q_{ref} \) \hspace{1cm} \text{the saturated reactive power reference, in p.u.}
\( v_e \) \hspace{1cm} \text{the equivalent internal voltage, in p.u.}
\( v_g \) \hspace{1cm} \text{the grid voltage, in p.u.}
\( V_{PCC} \) \hspace{1cm} \text{the PCC voltage magnitude, in p.u.}
\( v_{PCC} \) \hspace{1cm} \text{the PCC voltage, in p.u.}
\( v_{PWM} \) \hspace{1cm} \text{the voltage modulating signal, in p.u.}
\( V_{ref} \) \hspace{1cm} \text{the voltage magnitude reference, in p.u.}
\( V_t \) \hspace{1cm} \text{the inverter terminal voltage magnitude, in p.u.}
\( v_t \) \hspace{1cm} \text{the inverter terminal voltage, in p.u.}
\( v_{ref} \) \hspace{1cm} \text{the voltage reference generated by the outer loops, in p.u.}
\( \omega_{ref} \) \hspace{1cm} \text{the angular frequency reference, in rad/s}
\( X_T \) \hspace{1cm} \text{the transformer reactance, in p.u.}
\( Z \) \hspace{1cm} \text{the equivalent output impedance of the inverter, in p.u.}
\( Z_f \) \hspace{1cm} \text{the inverter filter impedance, in p.u.}
\( Z_{Fault} \) \hspace{1cm} \text{the fault impedance between the cable and the ground, in p.u.}
\( Z_{g1}, Z_{g2} \) \hspace{1cm} \text{the grid impedance, in p.u.}

I. INTRODUCTION

Grid-forming (GFM) inverter technology is treated as a promising solution for future bulk power systems with high penetration of renewable energy [1], [2]. Compared with grid-following (GFL) inverters, GFM inverters are controlled as voltage sources behind impedance during normal operation [3], [4]. Therefore, GFM inverters would be able to establish system voltage and frequency autonomously [5], and contribute to system strength [6].

The voltage source behavior of GFM inverters makes their current outputs highly dependent on external system conditions. Upon disturbances or faults, synchronous generators (SGs) can supply 5–7 p.u. fault current outputs [7]. In contrast, semiconductor-based inverters can only handle 0.2–1 p.u. over-current typically [8], [9], which prevents them from maintaining the voltage profile as in normal operation [10]. To maintain power system security, appropriate current-limiting control methods are required for GFM inverters, which satisfy the following requirements [11]–[15]:

- **Current limitation**: The GFM inverter’s output current magnitude must be lower than the maximum allowed limit, e.g., 1.2–2 p.u., to protect the semiconductor devices.
- **Fault ride-through (FRT) capability**: The GFM inverter should be able to ride through power system disturbances or faults, e.g., the voltage at the point of common coupling (PCC) drops to 0 for 140 ms or its phase jumps by 60 degrees [13].
- **Fault current injection**: The GFM inverter should supply the required active/reactive currents to support the power grid during disturbances or faults, e.g., inject positive-sequence reactive current within 5 ms after the PCC voltage falls below 0.9 p.u. [12], [13], or additional negative-sequence reactive current proportional to the negative-sequence voltage drops [14], [15].

To achieve these requirements, various current-limiting controls of GFM inverters are investigated in the literature. This paper reviews these methods and discusses future issues that need to be addressed based on stability requirements. An overall GFM control structure with current-limiting controls is derived, based on which different current-limiting methods are compared. Their advantages and disadvantages are also

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summarized. Finally, open issues still need to be resolved are discussed.

The remainder of this paper is organized as follows: Section II gives the basics of current-limiting controls for GFM inverters. In Section III, different current-limiting methods are reviewed and summarized. Open issues related to the power system requirements are discussed in Section IV. Finally, Section V concludes this paper.

II. BASICS OF CURRENT-LIMITING CONTROL METHODS

Fig. 1 shows a simplified circuit model of a grid-tied GFM inverter. The GFM inverter consists of an internal voltage source $v_e$ and equivalent output impedance $Z_e$.

According to the Kirchhoff’s circuit laws, the output current magnitude of the GFM inverter can be expressed as

$$I = ||i|| = \frac{||v_e - v_{PCC}||}{||Z_e + jX_f||}$$  \hspace{1cm} (1)

where $|| \cdot ||$ denotes the modulus of a complex variable, $j$ is the unit imaginary number. When a fault causes PCC voltage drop or phase angle jumps, the voltage difference $||v_e - v_{PCC}||$ can increase. Consequently, $I$ may exceed the maximum allowed value $I_M$ of the GFM inverter.

To prevent the GFM inverters from this dangerous situation, various current-limiting control strategies have been proposed in the literature [16], [17]. Based on whether the output current magnitude $I$ is directly or indirectly controlled, these strategies can be classified into three types:

1) Direct current-limiting control: GFM control systems directly restrict the output current magnitude $I$ within the maximum allowed value $I_M$ through current limiters [18]–[20] or power limiters [21], [22].

2) Indirect current-limiting control: GFM control systems indirectly restrict the output current magnitude $I$ by reducing the voltage difference $||v_e - v_{PCC}||$ through voltage limiters [23]–[25] or increasing the equivalent output impedance $||Z_e||$ based on virtual impedance/admittance [26]–[28].

3) Hybrid current-limiting control: GFM control systems restrict the output current magnitude $I$ through a combination of the direct/indirect current-limiting controls [29], [30].

In the next section, detailed implementation of these methods will be illustrated.

III. GFM INVERTER WITH CURRENT-LIMITING CONTROLS

Fig. 2 illustrates a generalized control diagram of a GFM inverter with current-limiting controls, where two main control loops are identified, i.e., the outer control loop and the inner one.

The main objective of the former is to synchronize the GFM inverter with the power grid and regulate the terminal voltage magnitude. A voltage magnitude $E$ and phase angle $\theta$ will be generated based on the active/reactive power references $P_{ref, Q_{ref}, \omega_{ref}}$, and the feedback signals $i$, $i_e$, $v_t$, $v_{PCC}$. The inner control loops aim to produce the voltage modulating signal $v_{PWM}$ from $v_{ref}$ generated by the outer control loop, which may not be needed for GFM controls [4]. The principles of direct and indirect current-limiting control methods are discussed in the following sections.

A. Direct Current-Limiting Control

As illustrated in Section II, the direct current-limiting control of GFM inverters can be achieved by current or power limiters. As noted in Fig. 2, the current limiters are usually implemented in inner control loops, while the power limiters are achieved in outer ones.

Current limiter: Three current limiters are commonly utilized for GFM inverters, including the instantaneous limiter [18], [31]–[33], the magnitude limiter [19], [34]–[37], and the priority-based limiter [20], [38]–[40]. As shown in Fig. 2, the main objective of the current limiters is to restrict the original current reference $i_{ref}$ to a saturated one $\tilde{i}_{ref}$ satisfying $||\tilde{i}_{ref}|| \leq I_M$. Thereafter, a high-bandwidth current regulator is utilized to realize $i = \tilde{i}_{ref}$, and thus $I \leq I_M$.

§ Instantaneous limiter

The illustration of an instantaneous limiter is shown in Fig. 3, which utilizes a element-wise saturation function to achieve a saturated current reference $\tilde{i}_{ref}$. The instantaneous limiter can be implemented in difference reference frames. In the natural reference frame (abc-frame), the instantaneous limiter is expressed as [31], [32]

$$\tilde{i}_{ref, x} = \begin{cases} I_M \text{sign}(i_{ref, x}), & |i_{ref, x}| > I_M \vspace{0.2cm} \\ i_{ref, x}, & |i_{ref, x}| \leq I_M \end{cases}, \ x = a, b, c. \hspace{1cm} (2)$$

In the stationary reference frame (αβ-frame) or the synchronous reference frame (dq-frame), the instantaneous limiter becomes [18], [33], [36]

$$\tilde{i}_{ref, x} = \begin{cases} I_{M, x} \text{sign}(i_{ref, x}), & |i_{ref, x}| > I_{M, x} \vspace{0.2cm} \\ i_{ref, x}, & |i_{ref, x}| \leq I_{M, x} \end{cases}, \ x = d, q/\alpha, \beta \hspace{1cm} (3)$$

where the current limit $I_{M, x}$ is selected as $I_M/\sqrt{2}$ to ensure that $\sqrt{i_{ref, d/\alpha}^2 + i_{ref, q/\beta}^2} \leq I_M$.

§ Magnitude limiter

The illustration of a magnitude limiter is given in Fig. 4(a), which only decreases the magnitude of the original current reference $i_{ref}$. The angle of $\tilde{i}_{ref}$ maintains the same as that of $i_{ref}$.

The magnitude limiter is originally designed in the αβ-frame or dq-frame, which is expressed as [19], [34], [35]

$$\tilde{i}_{ref} = \begin{cases} i_{ref}, & |i_{ref}| \leq I_M \vspace{0.2cm} \\ \frac{i_{ref}}{|i_{ref}|} i_{ref}, & |i_{ref}| > I_M \end{cases}. \hspace{1cm} (4)$$
Fig. 2. Control diagram of a GFM inverter with current-limiting controls.

Fig. 3. Illustration of an instantaneous limiter.

Fig. 4. Comparison of different current limiters: (a) magnitude limiter; (b) priority-based limiter.

In [36], [37], a generalized magnitude limiter is designed in the abc-frame as follows

\[ \tilde{i}_{\text{ref},x} = \begin{cases} i_{\text{ref},x}, & \text{if } i_{\text{ref},x} \leq I_M \\ \frac{I_M}{i_{\text{ref},x}}i_{\text{ref},x}, & \text{if } i_{\text{ref},x} > I_M \end{cases} , \quad x = a, b, c \tag{5} \]

where \( i_{\text{ref},x} \) represents the magnitude of \( i_{\text{ref},x} \).

§ Priority-based limiter

Fig. 4(b) shows the principle of the priority-based limiter, which not only decreases the magnitude of \( i_{\text{ref}} \) but also prioritizes its angle to a specific value \( \phi_I \). Notice that \( \phi_I \) is a user-defined angle that represents the angle difference between \( \tilde{i}_{\text{ref}} \) and the d-axis oriented to \( \theta \).

The priority-based limiter implemented in the dq-frame is represented as [20], [38]–[40]

\[ \tilde{i}_{\text{ref}} = \begin{cases} i_{\text{ref}}, & \|i_{\text{ref}}\| \leq I_M \\ \frac{I_M}{\|i_{\text{ref}}\|}i_{\text{ref}}, & \|i_{\text{ref}}\| > I_M \end{cases} \tag{6} \]

In [20], [39], \( \phi_I = 0 \) is selected. Further, \(-\pi/2 < \phi_I \leq 0\) is chosen in [40] based on an optimized method.

§ Comparison of different current limiters

Among the three current limiters, the instantaneous limiter is the simplest one to achieve the self-protection of GFM inverters. However, due to the clipping of the original current reference, the current outputs will no longer be sinusoidal [36]. Besides, as shown in (3), in the \( \alpha\beta \)-frame and \( dq \)-frame, conservative current limits are selected, which can reduce the capacity utilization of the GFM inverter and requires the use of inverters with a relatively large \( I_M \), e.g., 2 p.u. in [18], [33].

Compared with the instantaneous limiter, the magnitude limiter can ensure a sinusoidal current output \( i \) with extra current magnitude calculations. However, when it is implemented in the \( \alpha\beta \)-frame or \( dq \)-frame, the GFM inverter will suffer from over-voltage issues during asymmetrical faults, which can be avoided by implementing the magnitude limiter in the \( abc \)-frame [36]. Moreover, the angle of the saturated current reference \( \tilde{i}_{\text{ref}} \) is determined by the voltage regulator or virtual admittance control loops as shown in Fig. 2. The angle difference between \( i \) and \( v_I \) is not specified. Under faults or disturbances, extra control actions may be required to satisfy the fault current injection requirement [13], such as combining power limiters to form hybrid current-limiting controls [41]–[43], which will be discussed in Section III-C.

The same problem exists in GFM inverters [20], [39] with priority-based limiters since the relationship between \( i \) and \( v_I \) is dependent on the grid conditions and outer control loops. To satisfy the fault current injection requirement, one solution is to switch the GFM inverter to a voltage-synchronized GFL inverter when the priority-based limiter is triggered [38], [44]. Therefore, the injected active/reactive current can be fixed by tuning \( \phi_I \). However, the GFL inverters can suffer from small-signal or transient instability issues under weak grid conditions [45], [46]. An alternative solution that avoids switching the synchronization methods is the same as that of the magnitude limiter, i.e., utilizing a power limiter as illustrated in Section III-C.

Besides, instability issues have been recognized and analyzed for the instantaneous limiter [47], the magnitude limiter...
and the priority-based limiter [49] during faults or severe disturbances, which can prevent the GFM inverter from a successful FRT. In [50], the transient instability issue of priority-based limiter is alleviated by freezing the changing rate of \( \theta \). In [40], an optimized priority-based limiter is proposed to improve the transient stability margin of the GFM inverter.

Furthermore, according to Fig. 2, the saturation of the control signal \( i_{ref} \) requires appropriate anti-windup designs for the voltage regulator or virtual admittance control loops. Since the output current magnitude is directly controlled to be lower than \( I_M \), extra control may be required to switch the GFM inverter from the current-limiting mode to normal operation. For example, in [51], the hybrid synchronization control is utilized for GFM inverters with priority-based limiters to achieve a successful fault recovery.

**Power limiter:** As shown in Fig. 2, a power limiter is implemented in the outer loops [21], [22], [52], [53], which restricts the original power references \( P_{ref} \) and \( Q_{ref} \) to saturated ones \( \bar{P}_{ref} \) and \( \bar{Q}_{ref} \) satisfying \( \sqrt{P_{ref}^2 + Q_{ref}^2} \leq V_i I_M \) with \( V_i = ||v_i|| \). Thereafter, \( I \leq I_M \) is ensured when these power references are achieved by outer control loops, i.e., \( P = \bar{P}_{ref} \) and \( Q = \bar{Q}_{ref} \).

A power limiter is illustrated in Fig. 5. In normal operation, the power limiter is transparent. When fault or disturbance occurs, the saturated power references are usually selected based on grid codes [21], [22]. An example based on [13] is given as

\[
\bar{Q}_{ref} = \begin{cases} 
Q_{ref}, & V_{PCC} \geq 0.9 \text{ p.u.} \\
V_i I_Q, & 0.5 \text{ p.u.} < V_{PCC} < 0.9 \text{ p.u.} \\
V_i I_M, & 0 \leq V_{PCC} \leq 0.5 \text{ p.u.}
\end{cases}
\]  

(7)

and

\[
\bar{P}_{ref} \leq \sqrt{V_i^2 I_M^2 - \bar{Q}_{ref}^2}
\]  

(8)

where \( V_{PCC} = ||v_{PCC}|| \). \( I_Q \) denotes the reactive current requirement of the power grid when the PCC voltage is between 0.5 p.u. and 0.9 p.u. Thereafter, the saturated power references are achieved by proportional-integral controllers [22] or virtual oscillator controls [52], [53]. In [54], gradient terms are utilized to dynamically adjust the original power references.

Since the power references during faults can be set based on grid codes, the power limiter can achieve the steady-state fault current injection requirement. However, for GFM inverters, the control bandwidth of the outer control loops is usually designed to be much smaller than 50 Hz [55]. If the power limiter is used solely for current limitation, the GFM inverter can still suffer from over-current issues during transients.

**B. Indirect Current-Limiting Control**

The indirect current-limiting control methods are achieved by virtual impedance/admittance control methods or voltage limiters. As shown in Fig. 2, these methods modifies the voltage reference generated by the outer loops to realize current limitation.

**Virtual impedance/admittance:** Three typical implementation methods of the virtual impedance/admittance control are reviewed and demonstrated in Fig. 6. The corresponding equivalent circuit diagrams of these methods are given in Fig. 7.

\[ § Virtual impedance with inner loops \]

The virtual impedance with inner control loops is implemented in [26], [27], [56]–[60] for current limitation. Assuming that \( v_i = v_{ref} \) can be fast achieved by inner control loops, an equivalent circuit diagram of this method is demonstrated in Fig. 7(a).

In this method, the virtual impedance is added to \( v_{ref} \) when the output current magnitude \( I \) is greater than a certain threshold \( I_{thres} \), i.e.,

\[
\begin{cases} 
R_v = X_v = 0, & I \leq I_{thres} \\
||R_v + jX_v|| > 0, & I > I_{thres}
\end{cases}
\]  

(9)

with \( R_v \) and \( X_v \) being the virtual resistance and reactance, respectively.

There exist multiple other selection methods for \( R_v \) and \( X_v \), they can be either fixed [26], state-dependent [27], [56]–[59], or time-varying [60]. A typically state-dependent selection method for \( R_v \) and \( X_v \) is expressed as follows [27], [56]–[58]

\[
X_v = \sigma R_v, \quad R_v = \begin{cases} 
0, & I \leq I_{thres} \\
K_{V1}(I - I_{thres}), & I > I_{thres}
\end{cases}
\]  

(10)
where $\sigma$ is a user-defined $X/R$ ratio for the virtual impedance, $K_{VI}$ is a constant that satisfies
\[
\|R_v + jX_v\|_\infty = K_{VI} \sqrt{\sigma^2 + 1} (I_M - I_{thres}) \geq \frac{V_{\text{max}}}{I_M}
\]  
with $V_{\text{max}}$ being the maximum voltage difference between $Ee^{j\theta}$ and $v_i$. Note that $\|R_v + jX_v\|_\infty \geq V_{\text{max}}/I_M$ with $I = I_M$ is also a parameter selection requirement for all existing methods.

§ Virtual impedance without inner loops

The virtual impedance without inner control loops is presented in [28], [61], whose equivalent circuit diagram is demonstrated in Fig. 7(b).

Notice that in this method, the virtual impedance is directly added to the modulating signal $v_{PWM}$ when the output current magnitude $I$ is greater than $I_{thres}$.

Different from the previous method, the inverter filter will be in series with the virtual impedance as shown in Fig. 7(b) since no inner control loops are involved in the virtual impedance control [62], [63]. Again, $R_v$ and $X_v$ are selected as fixed [28] or state-dependent [61] values similarly to (11), satisfying
\[
\|R_v + jX_v + Z_f\|_\infty \geq \frac{V_{\text{max}}}{I_M}, \quad I = I_M.
\]  

§ Virtual admittance

The virtual admittance control method shown in Fig. 6(c) is applied in [64], [65] for current limitation. With a high-bandwidth current regulator, the corresponding equivalent circuit diagram is given in Fig. 7(c).

Unlike the previous virtual impedance methods whose $R_v$ and $X_v$ can be set to zero when $I \leq I_{thres}$, the virtual admittance method cannot have $R_v = L_v = 0$ in normal operation, where $L_v$ denotes the virtual inductance. Therefore, the virtual admittance is selected as [64], [65]
\[
R_v = \max\{R_{vn}, Z_v/\sqrt{\sigma^2 + 1}\}
\]
\[
L_v = \max\{L_{vn}, \sigma R_v/\omega_n\}
\]  
(13)

where $Z_v = \|Ee^{j\theta} - v_i\|/I_M$, $R_v$ and $L_{vn}$ are the virtual admittance parameters in normal operation, $\omega_n$ is the nominal angular frequency.

§ Comparison of different virtual impedance/admittance methods

Compared with the virtual admittance method that can achieve a virtual inductance $L_v$ within the bandwidth of the current regulator, the virtual impedance method requires a derivative controller to achieve $L_v$ [28] or uses an virtual reactance $X_v$ at the nominal frequency as mentioned above.

Besides, the virtual impedance method with inner control loops achieves current limitation based on the hypothesis that the voltage reference $v_{ref}$ can be achieved by the inner control loops. Due to the relatively low bandwidth of the voltage regulator [66], temporary over-current may be observed [67]. In comparison, the virtual impedance method without going through inner control loops directly modifies the modulating signal based on feeding back current outputs, which is able to avoid over-current for the first cycle when fault occurs [30].

To achieve effective current limitation with the virtual impedance methods, the control parameters $R_v$ and $X_v$ ($L_v$) are highly dependent on the considered worst case, i.e., $V_{\text{max}}$, which introduces a tradeoff between current-limiting performance and stability. On one hand, when using a small $V_{\text{max}}$, the output current magnitude $I$ cannot be ensured to be within $I_M$ when $\|Ee^{j\theta} - v_i\|$ is larger than $V_{\text{max}}$. On the other hand, when using a large $V_{\text{max}}$, according to (11), large $R_v$ and $X_v$ will also be applied, which can induce small-signal or transient instability issues [57], [68].

One main advantage of the virtual impedance/admittance methods is that they will not introduce windup problems to the inner control loops, which relax the requirement of extra mode-switching mechanisms [69], [70]. However, anti-windup methods may still be required for outer control loops.

Voltage limiter: Voltage limiters aim to directly reduce the voltage difference $\|v_{PWM} - v_i\|$ to be smaller than $\|Z_f\|/I_M$ [23], [24], [71], [72]. This method is a preferred solution in industry since it does not require adaptive virtual impedance that can destabilize the system under certain conditions [73].

According to Fig. 2, the current output satisfies $I = \|v_{PWM} - v_i\|/\|Z_f\| \leq I_M$. In these methods, the inner
control loops are commonly transparent, i.e., \( v_{PWM} = v_{ref} \). Subsequently, an equivalent circuit diagram of this current-limiting method is given in Fig. 8.

The implementation of the voltage limiter is usually achieved by regulating \( E \) and \( \theta \) generated by the outer control loops, expressed as [23], [24]

\[
\|v_{ref}\| = \begin{cases} 
V_t + E_{\text{lim}}, & E > V_t + E_{\text{lim}} \\
E, & V_t - E_{\text{lim}} \leq E \leq V_t + E_{\text{lim}} \\
V_t - E_{\text{lim}}, & E < V_t - E_{\text{lim}}
\end{cases}, \quad (14)
\]

and

\[
\arg(v_{ref}) = \begin{cases} 
\theta_t + \delta_{\text{lim}}, & \theta > \theta_t + \delta_{\text{lim}} \\
\theta, & \theta_t - \delta_{\text{lim}} \leq \theta \leq \theta_t + \delta_{\text{lim}} \\
\theta_t - \delta_{\text{lim}}, & \theta < \theta_t - \delta_{\text{lim}}
\end{cases}, \quad (15)
\]

where \( \theta_t \) is the phase angle of \( v_t \), \( E_{\text{lim}} \) and \( \delta_{\text{lim}} \) are maximum allowed magnitude difference and angle difference, respectively. In [23], [24], these parameters are selected to ensure that \( \|v_{ref} - v_r\| \leq \|Z_f\|I_M \).

In [25], [71], the saturated voltage reference is generated by \( v_{ref} = v_t + Z_f I_M e^{j\phi_t} \) with \( \phi_t \) being the same as the pre-fault angle of \( i \). In [72], a voltage limiter is directly designed in the abc-frame where the voltage limits are calculated for each phase.

As illustrated above, the voltage limiter in may not need the information of \( i \) as the other current-limiting methods. However, it requires extra information of the terminal voltage \( v_t \), such as its phase angle [23] and magnitude [24].

Besides, appropriate anti-windup designs for outer loops are required due to the saturation of the control signals \( E \) and \( \theta \). When both \( E \) and \( \theta \) are saturated as in (14)-(15), the outer control loops will lose their controllability. The voltage reference \( v_{ref} \) has to follow the change of its terminal voltage \( v_t \). Consequently, the GFM inverter will become a voltage-synchronized inverter that may suffer from instability issues under weak grid conditions [45], [46].

In [24], only the magnitude \( E \) is saturated by the voltage limiter. The possible instability issues caused by voltage-based synchronization can be alleviated. However, current limitation cannot be always ensured, e.g., \( V_t |\sin(\theta - \theta_t)| > \|Z_f\|I_M \).

C. Hybrid Current-Limiting Control

In this section, hybrid current-limiting control methods are discussed to achieve better current limitation or fault current injection requirements.

Note that the virtual impedance methods have no windup issues as current limiters but its current-limiting performance is reduced compared with the current limiters. In order to combine the advantages of these two methods, hybrid current limiting methods that combine the virtual impedance with the current magnitude limiter [29] or the priority-based current limiter [67] are presented.

Moreover, the steady-state fault current injection requirement of grid codes can be achieved by power limiters. However, the current-limiting performance may be compromised. In [41]–[43], hybrid current-limiting methods that combine the power limiter and current magnitude limiter are proposed to improve the current-limiting performance and fault-current injection requirement, simultaneously. In [30], when no inner control loops are applied, the power limiter is combined with a designed virtual resistance control to achieve current limitation.

IV. OPEN ISSUES

In this section, issues related to current-limiting control of GFM inverters, including control stability, fault recovery, and fault current injection, are discussed.

A. Control Stability

For GFM inverters with current-limiting controls, transient stability is an essential requirement for both GFM inverter protection and successful FRT.

For certain faults or disturbances, numerical methods are widely applied to testify the stability of a single GFM inverter with current limiters [18], [19], [44], power limiters [21], [54], virtual impedance/admittance [27], [65], and hybrid methods [41], [42]. Furthermore, the stability and performance of multiple GFM inverters with different current-limiting methods are illustrated by the numerical methods in [20], [23], [33]–[36], [59]–[61], [74], [75].

Although all details of the inverter nonlinear dynamics can be included in the numerical methods for stability assessment, significant computational resources will be required for the stability analysis of a power grid with high penetration of GFM inverters. Moreover, the numerical simulations fail to shed analytical insights into the impacts of control loops.

Besides the numerical method, for a single GFM inverter, small-signal stability analysis is usually applied for different current-limiting control methods, such as priority-based limiters [38], power limiters [22], [52], virtual impedance [28], [57], voltage limiters [24], [72], and hybrid methods [29]. In addition to the small-signal stability analysis, nonlinear system theory is also used to analyze the stability of GFM inverters, such as bifurcation theory [47], Lyapunov theory [48], phase plane analysis [30], [40], [51], etc. The advantage of these theoretical methods is that they can guide the selection of control parameters. However, these results are hard to extend to the transient stability of multiple GFM inverters under faults or severe disturbances.

For a power grid with multiple GFM inverters, due to its complex dynamic model, transient stability is hard to be analyzed either theoretically or numerically. One possible way is to develop simplified models for GFM inverters with sufficient details describing the stability behavior in the considered timescale. Usually, a GFM inverter with limited current output can be modeled as a synchronized current source with fixed or state-dependent output current magnitude or a synchronized voltage source with a nonlinear time- or state-dependent output impedance. The selection of different models in different scenarios may facilitate the transient stability analysis.

B. Fault Recovery

A successful FRT process requires that GFM inverters should be able to restore their normal operation from the
current-limiting mode when faults or disturbances are clear [55].

One main challenge in fault recovery is caused by the windup of different control loops. For example, as shown in Fig. 2, when current limiters are applied and triggered, the inverter terminal voltage cannot track its reference anymore, leading to the windup of voltage integrators. The magnitude of the generated current reference can be always larger than $I_M$. Consequently, the current limiter is always active, which prevents the GFM inverter from a successful fault recovery [31], [51], [57]. Additionally, as discussed in Section III-B, the windup issues of inner control loops can be alleviated by the virtual impedance/admittance methods. However, when faults or disturbances occur, the inverter terminal voltage has to drop to reduce the inverter current output [10]. Therefore, voltage magnitude regulators may still suffer from the windup issues.

To approach the fault recovery issues induced by controller windup, appropriate anti-windup methods should be selected for GFM inverters. In addition to the commonly used methods, such as back-calculation, clamping, etc., novel anti-windup algorithms for different current-limiting controls may be developed to help GFM inverters recover from current limitations. Note that it is important to evaluate their effectiveness under different faults or disturbances.

C. Fault Current Injection

Fault current injection is originally proposed for GFL inverters under symmetric [12] or asymmetric faults [14], [15], which aims to provide the power grid with positive/negative-sequence voltage support. For GFL inverters, this requirement can be satisfied by setting the active/reactive current references according to grid codes under either symmetric or asymmetric faults [76]. For GFM inverters, as mentioned previously, the fault current injection requirement can be met by changing the GFM inverter to a GFL one during faults or disturbances [38], [44], [77], [78], and another solution is to change the power references through a power limiter [30], [41], [43].

Notice that there is a conflict between maintaining the voltage source behavior of GFM inverters and the precise control of its output current phase angle [10]. Under grid faults or disturbances, the former is more demanded than the fault current injection requirement. In a recently implemented grid code [13], a new fault current injection requirement is proposed, which needs GFM inverters to have a faster current response than that of GFL inverters. More specifically, the GFM inverter should begin to inject reactive current to the power system in less than 5 ms when the PCC voltage drops below 0.9 p.u. In such a small timescale, it may be difficult to realize this requirement by closed-loop current/power controls.

Instead of directly controlling the current/power outputs of the GFM inverter, keeping the voltage source behavior of GFM inverters during faults or disturbances with a natural current response seems to be a viable solution [10], [13]. Next, the control system can adjust the power references based on grid codes to maintain and regulate the injected fault current. Further evaluations of this solution and the corresponding theoretical analysis are needed.

Additionally, in conventional transmission systems, the protection relays such as distance relays, differential relays, etc. are commonly designed based on the fault current characteristics of the SGs [9]. However, the fault current characteristics of the GFM inverters will be mainly determined by their current-limiting control methods [79], making the protection relays less reliable [80]. Proper coordination methods between the GFM inverters with current-limiting controls and the protection relays are required.

V. Conclusion

This paper presents a review of the existing current-limiting control methods for grid-forming (GFM) inverters and summarizes open issues related to these methods. Based on whether the current output is controlled directly or not, current-limiting controls are classified as direct, indirect, or hybrid ones. Further, a general control diagram of a GFM inverter with current-limiting controls is presented to illustrate the implementation of these methods, including current limiters, power limiters, virtual impedance/admittance control, and voltage limiters. Their advantages and disadvantages regarding the current-limiting performance, fault ride-through (FRT) capability, and satisfaction of fault current injection requirement are demonstrated. Finally, open issues related to control stability, fault recovery, and fault current injection are discussed.

REFERENCES


