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October 30, 2023

Abstract

We report a vertical β-Ga2O3 Schottky Barrier Diode (SBD) with BaTiO3 as field plate oxide on low doped thick epitaxial layer exhibiting 2.1 kV breakdown voltage. A thick drift layer of 11 μm with a low effective doping concentration of $8 \times 10^{15}$ cm$^{-3}$ is used to achieve high breakdown voltage. Using the high-k dielectric with dielectric constant of 248, the breakdown voltage increases from 816V for the non-field-plated SBD to 2152V (>2x improvement) for the field-plated SBD without compromising the on-state performance. The diode dimensions are varied to analyze the effect of edge high-field related leakage with reverse bias and also the effect of current spreading during forward operation. Very uniform distribution of breakdown voltages of 2152V±20V are observed for the diode diameters from 50 μm to 300 μm for the field-plated SBDs. The on and off state power losses are also analyzed and compared with the non-field-plated devices and the switching losses are estimated analytically.
2.1 kV (001)-$\beta$-Ga$_2$O$_3$ Vertical Schottky Barrier Diode with High-k Oxide Field Plate

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(Dated: 7 December 2022)

We report a vertical $\beta$-Ga$_2$O$_3$ Schottky Barrier Diode (SBD) with BaTiO$_3$ as field plate oxide on low doped thick epitaxial layer exhibiting 2.1 kV breakdown voltage. A thick drift layer of 11 $\mu$m with a low effective doping concentration of $8 \times 10^{15}$ cm$^{-3}$ is used to achieve high breakdown voltage. Using the high-k dielectric with dielectric constant of 248, the breakdown voltage increases from 816V for the non-field-plated SBD to 2152V (>2x improvement) for the field-plated SBD without compromising the on-state performance. The diode dimensions are varied to analyze the effect of edge high-field related leakage with reverse bias and also the effect of current spreading during forward operation. Very uniform distribution of breakdown voltages of 2152V±20V are observed for the diode diameters from 50 $\mu$m to 300 $\mu$m for the field-plated SBDs. The on and off state power losses are also analyzed and compared with the non-field-plated devices and the switching losses are estimated analytically.

$\beta$-Ga$_2$O$_3$ has emerged as the material for the next generation power electronics due to its ultra-wide bandgap of 4.6-4.8 eV and high critical electric field strength$^1$ resulting in a power figure of merit (PFOM) higher than wide bandgap materials such as SiC and GaN. The availability of high-quality melt grown bulk substrates also results in superior epitaxial layer growth$^2$ and potentially reduced cost. The rapid advances in materials development also enabled many of the state of the art device realization in both vertical and lateral geometry (HVPE) are commercially available with less than 10$^{16}$ cm$^{-3}$ doping concentration which is highly promising for the development of multi-kilovolt class vertical devices.

Despite all the progress in materials development, $\beta$-Ga$_2$O$_3$ poses some fundamental challenges which restrict the devices from achieving the full potential. In any power devices, electric fields crowd near the device edges and corners at high reverse bias$^{17}$ which causes the premature breakdown of the devices and these edge field crowding need to be managed to maximize the blocking performance. p-type guard rings are widely employed as edge terminations in Si$^{18}$ and SiC$^{19}$ based power devices which significantly enhances device performance. The lack of p-type doping in $\beta$-Ga$_2$O$_3$ prevents using such approaches and poses fundamental challenges in device design. Alternative approaches have been explored over the years to address the issue of edge terminations in $\beta$-Ga$_2$O$_3$ based devices$^{5,20,21}$. Field plating is one such edge termination technique which is used in $\beta$-Ga$_2$O$_3$ based devices to reduce electric field crowding near device edges and corners. However, the effect of the field-plating depends heavily on the dielectric material that is used as field-plated devices would be limited by the dielectric breakdown if poor quality dielectrics are used. Low-k dielectric such as SiO$_2$ or Al$_2$O$_3$ can provide high-breakdown field but the breakdown is still limited by the breakdown at the dielectric edge. High-k dielectric on the other hand drops very less electric field within it and can spread the electric field more efficiently compared to low-k dielectrics$^{8,22}$. We have demonstrated the effect of high-k dielectric as field plate oxide in $\beta$-Ga$_2$O$_3$ based SBDs achieving a breakdown voltage of 687V on a thin (1.7 $\mu$m) drift layer$^{23}$. Due to the thin drift layer used the breakdown voltage was limited to less than 1kV. In this work we have used a thick (11 $\mu$m) low doped ($5 \times 10^{15}$ cm$^{-3}$) drift layer to achieve breakdown voltage of more than 2 kV. The device breakdown uniformity is measured on SBDs with different diameters. The leakage through the high-k dielectric was also characterized in both forward and reverse conditions. The power loss also is determined and compared with the non-field-plated devices.

The SBDs as shown in Fig. 1(a) were fabricated on 11 $\mu$m thick drift layers grown using halide vapor phase epitaxy on (001) conductive substrates (NCT Japan). Standard solvent clean (Acetone/Methanol/DI water) was performed before device fabrication. After solvent cleaning 300 nm thick BaTiO$_3$ was deposited using RF sputtering at room temperature in oxygen ambient with O$_2$/Ar ratio of 1:10 and at a sputter power of 140W and chamber pressure of 5mTorr$^{12,23}$. A-
FIG. 2. Forward current voltage characteristics for the field-plated SBDs for different diode diameters in (a) linear and (b) log scale. (c) $R_{on-sp}$ vs diode diameter for the field-plated SBD showing increase in $R_{on-sp}$ with diode diameter (d) Current voltage characteristics for the BTO MOSCAP showing negligible current density in diode operating voltage (0-2V)

ter the dielectric deposition, the samples were annealed at 700 °C in oxygen ambient for 30 minutes to enhance the dielectric constant. The sample was then patterned using standard photolithography and active regions of five different diameters were defined. BaTiO$_3$ is then removed from the active regions using BCl$_3$/Ar based ICP RIE. For the fabrication of control devices, BaTiO$_3$ is removed completely from half of the sample. Pt/Au (50/100 nm) Schottky contacts of five different diameters were then deposited using electron beam evaporation. For the field-plated devices, the Schottky metals were extended 25 µm over the BaTiO$_3$ layer. Finally, Ti/Au (50/100 nm) ohmic contacts were sputter deposited on the back side of the sample.

Using capacitance voltage (CV) measurements on the regular SBDs as shown in Fig. 1(b), very low net doping concentration ($N_D-N_A$) of $8\times10^{15}$ cm$^{-3}$ was extracted. The dielectric constant of the sputtered BaTiO$_3$ layer is estimated by comparing the capacitance values at zero bias as shown in Fig. 1(b), yielding a dielectric constant of 248.

Current voltage (IV) characteristics for the field-plated SBDs with different diameters in logarithmic and linear scale are shown in Fig. 2(a) and (b). A Schottky barrier height of 1.3 eV and an ideality factor ($n$) of 1.03 was extracted using thermionic emission model indicating negligible damage to the Schottky interface due to dry etching. The specific on resistance ($R_{on-sp}$) for the diodes are extracted to be 6.9-8.7 mΩ-cm$^2$ for the field-plated SBDs. The $R_{on-sp}$ is found to be decreasing with increasing diode diameter ($D_A$) which indicates that a significant amount of current spreading in smaller diameter diodes. In Fig. 2(c), the dependence of $R_{on-sp}$ on diode diameter is shown with and without current spreading (A 45° spreading angle is considered as shown in the inset of Fig. 2(c)). It can be seen that if current spreading is considered, the $R_{on-sp}$ becomes independent on diode diameter. The current through the BaTiO$_3$ layer is also found to be negligible at the operating voltage (0-2V) as can be seen in Fig. 2(d), where the measurements have been performed on the MOS capacitors.

Reverse IV characteristics for the field-plated and non-field-plated SBDs are shown in Fig. 3(a). The breakdown voltage of the field-plated diodes are extracted to be $\sim771$-816V, whereas the field-plated SBDs exhibit very high breakdown voltage of $\sim2134$-2186V with no significant variation with respect to the diode diameter. The breakdown is also found to be catastrophic for both the non-field-plated and field-plated SBDs. The leakage current density at breakdown is found to be decreasing with diode diameter which indicates that the leakage current is mainly flowing through the device periphery. If the currents are normalized to the device periphery ($\pi D_A$) instead of total area, the leakage current is found to be much uniform over the diode diameter as shown in Fig. 3(b), which confirms that the a significant amount of leakage currents are mainly flowing through the device edges instead of the total device area. Negligible current is found to flow through the high-k dielectric upto 2kV as shown in Fig. 3(c).

The electric field simulations for the non-field-plated and field-plated SBD structures are also performed using Sentaurus TCAD software$^{24}$ and results are plotted in Fig. 4(a) and (b). Both of the diodes reach punchthrough field profile at breakdown condition, where punchthrough voltage is estimated to be $\sim729$V. The surface electric field at breakdown voltage reaches 1.5 MV/cm for the non-field-plated SBD and 2.6 MV/cm for the field-plated SBD. A peak electric field of 8-9 MV/cm was estimated at anode edges suggesting the lo-
state power losses respectively and D is the duty cycle. 

$$P_{Loss} = D \times P_{On} + (1 - D) \times P_{Off} + E_{sw} \times f_{sw}$$  \hspace{1cm} (1)$$

where, $P_{Loss}$, $P_{On}$, and $P_{Off}$ are the total, On state and off state power losses respectively and D is the duty cycle. $E_{sw}$ and $f_{sw}$ are the switching energy loss and switching frequency respectively.

Firstly, the static power losses are estimated using $P_{On}=V_{On}J_{On}$ and $P_{Off}=V_{BR}J_{BR}$. $V_{On}$ is defined as the voltage at $J_{On}=100 \, \text{A/cm}^2$ which is around 1.7V and 1.73V for the non-field-plated and field-plated SBDs respectively. $V_{BR}$ is the breakdown voltage and $J_{BR}$ is the leakage current at the breakdown voltage. For a fair comparison, $V_{BR}$ of $\sim$816V is considered for both the non-field-plated and field-plated SBDs and $J_{BR}$ is $\sim$8.9 mA/cm$^2$ and $\sim$0.5 µA/cm$^2$ for the non-field-plated and field-plated SBDs respectively.

The on state power loss for the field-plated and non-field-plated SBDs are approximately equal as shown in Fig. 5(a). However, the off state power loss is much higher for the non-field-plated SBDs compared to the non-field-plated SBD as the leakage current is much higher for the non-field-plated SBDs. However the total power loss is similar for both the non-field-plated and field-plated SBDs as it is dominated by the on-state power loss. Hence, the total static power loss for both the non-field-plated and field-plated SBDs are almost identical.

Now one major concern for adding high-k material is the increase in switching power loss due to the increase in capacitance. Hence, we estimated the switching power losses analytically to compare the field-plated and non-field-plated SBDs. The switching losses are estimated by considering total amount charge that needs to be removed or added while switching. Only capacitive charge storage is considered for the SBDs. Also, since both the non-field-plated and field-plated SBDs operate at punch-through condition at breakdown ($V_{P}$=729V, where $V_{P}$ is the punch through voltage), the energy loss for the non-field-plated SBD during switching can be estimated using (2),

$$E_{sw-nFP} = \frac{1}{2} C (V_{BR}^2 - V_{P}^2) = \frac{\varepsilon}{2L_{Drift}} (V_{BR}^2 - V_{P}^2)$$  \hspace{1cm} (2)$$

where, C is the capacitance per unit area, $\varepsilon$ is the dielectric constant of $\beta$-Ga$_2$O$_3$, and $L_{Drift}$ is the thickness of the drift layer. Now for field-plated SBD contains a Schottky region and a MOS region as shown in the inset of Fig. 5(b). Thus the total capacitance would be the combination of the Schottky depletion capacitance and MOS depletion capacitance. The MOS depletion capacitance per unit area can be approximated to be $\varepsilon_{Drift} \times \frac{\pi(R^2-r^2)}{\pi^2}$, where, $R$ is the outer circle radius and $r$ is inner circle radius. Here it is assumed that no voltage is dropped in the high-k dielectric and lateral depletion is ignored. Thus, total switching energy loss for the field-plated SBDs can estimated using (3),

$$E_{sw-FP} = \frac{1}{2} \left[ \frac{\varepsilon}{L_{Drift}} \left( \frac{R^2}{r^2} \right) \right] (V_{BR}^2 - V_{P}^2)$$  \hspace{1cm} (3)$$

The estimated switching power losses are plotted as a function of switching frequency in Fig. 4(b). It can be seen that if the field-plated SBDs are switched at 2.1kV compared to the 816 V of non-field-plated SBDs, switching power loss becomes significantly high ($\sim$26x) for the field-plated SBDs compared to the non-field-plated SBDs. However, if the field-plated and non-field-plated devices are switched at the same voltage, the switching power loss is almost identical for both the devices. It can also be seen that the switching power loss decreases with increase in diode diameter as the charge contribution of the MOS region to the total stored charge decreases. Thus, the adding of the high-k layer does not significantly increase the power loss compared to the bare Schottky devices.

In summary, we have reported 2.1kV rated high-k field-plated planar Schottky diodes with large diameters. The deposition of high-k dielectric and dry etching is found to have negligible effect on the forward characteristics of the diode. The breakdown voltage for the field-plated SBDs increases by $\sim$2.7x compared to the non-field-plated SBDs and the...
breakdown voltages are found to be very uniform over different Schottky diameters. The static and switching power losses for the SBDs are also analyzed and it has been found that the static power loss is almost identical for the non-field-plated and field-plated devices. The switching power loss is found to be almost identical for the the non-field-plated and the field-plated SBDs if both the devices are operated at the same reverse blocking voltage the total switching power loss decreases with increase in diode diameter. The addition of the high-k dielectric thus has negligible effect of the switching losses. Hence, the high-k field-plated devices can be operated at both high reverse voltage (2.1 kV)/low switching frequency (10 kHz) and low reverse voltage (800V)/high switching frequency (>100 kHz). Hence, the use of such high-k dielectric can more effectively utilize the high breakdown fields in ultrawide bandgap materials by proper electric field management and the true potential of these materials can be utilized for next generation power electronics.

ACKNOWLEDGMENTS

The authors acknowledge the funding from II-VI Foundation Block Gift Program and from the Air Force Office of Scientific Research under award number FA9550-21-0078. Any opinions, findings, conclusions or recommendations expressed in this article are those of the author(s) and do not necessarily reflect the views of the united states air force. A portion of this work was performed in the UCSB Nanofabrication Facility, an open access laboratory.

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