Comparative Analysis of Various Sinusoidal Pulse Width Modulation Techniques

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Abstract

This paper examines several sinusoidal pulse-width modulation (SPWM) methods for single-phase H-Bridge inverters. Various SPWM strategies have been proposed in the literature up to this point. With PWM, the inverter’s output voltage can be changed, so large filters are no longer needed. The conventional and modified SPWM techniques are described in this paper. Total Harmonic Distortion (THD), switching losses, fundamental component values, and dead time losses are used to compare the effectiveness of these SPWM methods. A MOSFET-based H-bridge inverter circuit is developed to verify different SPWM methods. The design of a transformer-based filter circuit for a single-phase H-bridge inverter is also included in this study. The hardware implementation uses the Delfino TMS320F28379d digital signal processor (DSP). This article explains how to integrate MATLAB-Simulink with the TMS320F28379D DSP processor. The hardware results, as well as the programming approach, are presented in this paper.
Comparative Analysis of Various Sinusoidal Pulse Width Modulation Techniques

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KEYWORDS
Bipolar, Efficiency, Hybrid, SPWM, THD, Unipolar

1 | INTRODUCTION

As power electronics technology advances, the reliance on renewable energy systems grows. In contrast to the conventional generator-based energy sources, these renewable energy sources (such as PV) are mostly inverter-interfaced
For off-grid and grid-connected systems, single-phase (half-bridge and full-bridge) or three-phase inverters are used depending on the load requirements. Single-phase full-bridge inverters are commonly used in integrated rooftop PV systems [2]. Electric vehicle/hybrid electric vehicle (EV/HEV) and uninterruptible power supply (UPS) systems also require inverter circuits. The inverter circuits’ frequency and output voltage are controlled using pulse width modulation (PWM) techniques [3].

Among various PWM methods, SPWM is extensively used because of its ease of implementation, cost-effective properties [3, 4, 5, 6] and lower harmonic content [7]. SPWM techniques can broadly be classified as bipolar [8, 9] and unipolar [4]. These traditional SPWM methods suffer from shortcomings like high total harmonic distortion (THD), high switching losses etc. A modified SPWM method is presented in [10] to reduce the THD value of the SPWM method. Modified bipolar SPWM [11] and modified unipolar SPWM methods [12, 13, 14] are introduced in the literature to reduce the THD and switching losses and increase the fundamental output of the inverter. The hybrid SPWM [15] method is introduced in the literature to reduce the switching losses of the inverter. In the case of modified bipolar, modified unipolar and hybrid SPWM methods, the switching losses for all the switches are unequal. This may result in unequal temperature rise among the switches. To overcome this shortcoming, a symmetrical hybrid SPWM method is presented in [16].

The lower-order harmonics of the inverter are filtered out by using SPWM techniques. To filter out the higher-order harmonics, low pass filters (LPF) are used for inverter circuits [17]. Instead of using a first-order L filter, the second-order L-C filters are recommended for their better performance [18]. With the increase in switching frequency of the SPWM technique, the high-frequency EMI (electromagnetic interference) noise also increases [19]. To reduce the harmonics and EMI noise, LCL, LLCL and LCL-LC filters are introduced in the literature [20]. The filter is designed based on the current, voltage and switching frequency of the inverter circuit. The filter design also depends on the SPWM method since the THD value differs for each SPWM method [21]. Instead of using an extra L-C filter, the system transformer can eliminate the higher-order harmonics [22].

The switching losses of the inverter are calculated based on the circuit operating conditions [23]. The switching loss occurs during the turn ON and turn OFF period [18] i.e. it depends upon the operating frequency of the inverter circuit. Total switching losses of the SPWM-controlled inverter depend upon the SPWM method as the operating frequency of the switch differs depending upon the control logic [16].

A dead time is provided among the switches from the same leg to avoid any short circuit condition [24]. This dead time causes voltage harmonics and current distortion in the inverter output [25]. The switching and dead time losses of the inverter circuit also change with the different SPWM methods.

Microcontroller-based digital control is widely used for SPWM control of inverters for its ease of implementation [6, 26]. This microcontroller-based digital control system has limitations in sample rate and multi-processing [27]. To overcome these limitations, FPGA (Field programmable gate array)/DSP (Digital Signal Processor) based controllers are gaining popularity in SPWM control applications [4]. This FPGA/DSP-based controller can ensure high-frequency switching operation, which minimizes the lower order harmonics [3]. The literature shows that the FPGA/DSP-based controller has robust control, though the implementation is complex compared to the microcontroller-based system [12, 28].

In this paper, various SPWM techniques are explained, and a comparison among these methods has been presented. This paper aims to compare these SPWM methods and find the technique with the least THD, switching loss, dead time loss and the highest fundamental component value. A MOSFET-based single-phase H-bridge inverter circuit has been developed for the experimental purpose. To reduce the implementation complexity of the DSP-based controller, MAT LAB-Simulink integration is proposed [29, 30]. This paper shows the implementation of MATLAB-Simulink integrated TMS320F2879d for the different SPWM methods.
FIGURE 1  Single Phase H-Bridge Inverter

The contributions to the work are:

a) The implementation and working of various SPWM methods are explained in this paper.
b) Different parameters to measure the inverter performance are explained.
c) The development of a transformer-based filter is presented in this paper.
d) The implementation of the SPWM method using DSP TMS320F28379d is presented in this article. MATLAB-Simulink is used to implement the SPWM logic.
e) A MOSFET-based inverter circuit is designed to verify the performance of different SPWM methods.

The paper is organized as follows: Section 2 explains the basics of the SPWM method along with its Fourier Transformation. Section 3 discusses different SPWM methods in the literature to date. Section 4 is dedicated to comparing the SPWM methods based on different performance parameters. Section 5 explains the development of a transformer-based filter circuit. The implantation of MATLAB-Simulink integrated TMS320F2879d for the SPWM method is explained in Section 6. Section 7 is dedicated to the hardware implementation of different SPWM methods. Section 8 concludes the paper.

2  |  BASICS OF SINUSOIDAL PULSE WIDTH MODULATION

A full-bridge single-phase inverter has four switches (AH, AL, BH, BL), as shown in Figure 1. The switching combination AH and BL are turned ON to provide a positive current to the load side, and the switching combination AL and BH are turned ON to provide a negative current to the load side. The selected PWM scheme controls the operation of the switches.

In the case of SPWM, a triangular carrier signal, \( V_{tr} \), (with a frequency of \( f_c \)), is compared with a sinusoidal waveform, \( V_{sin} \) (with a frequency of \( f_r \), equal to the output frequency) to determine the switching pattern, as shown in Figure 2a. The frequency modulation ratio can be expressed as,

\[
m_f = \frac{f_c}{f_r}
\]  

(1)
The modulation index can be expressed as,

\[ m_i = \frac{V_{\text{sin(peak)}}}{V_{\text{tri(peak)}}} \]  

(2)

The inverter output voltage can be expressed by a Fourier series [3] as,

\[ f(\omega t) = a_0 + \sum_{n=1}^{\infty} \left[ a_n \sin(n\omega t) + b_n \cos(n\omega t) \right] \]  

(3)

Where,

\[ a_0 = \frac{1}{2\pi} \int_{0}^{2\pi} f(\omega t) d(\omega t) \]

\[ a_n = \frac{2}{2\pi} \int_{0}^{2\pi} f(\omega t) \sin(n\omega t) d(\omega t) \]

\[ b_n = \frac{2}{2\pi} \int_{0}^{2\pi} f(\omega t) \cos(n\omega t) d(\omega t) \]

Due to odd wave \((f(\theta) = -f(\pi+\theta))\), and quarter wave symmetry \(f(90^\circ+\theta) = f(90^\circ-\theta), f(270^\circ+\theta) = f(270^\circ-\theta)\) of the waveform, here, \(a_0 = a_n = 0\) for all values of \(n\). In addition, \(b_n = 0\) for all even values of \(n\). For the odd values of \(n, b_n\) can be calculated for SPWM techniques.

3 | VARIOUS SPWM TECHNIQUES

3.1 | Bipolar SPWM

In this technique, \(V_{\text{tri}}\) is compared with \(V_{\text{sin}}\), as shown in Figure 2a. AH, BL and AL, BH operate in alternate with the frequency, \(f_{bi}\). A zero output voltage state does not exist in this method, as shown in Figure 2b. Here, the frequency modulation ratio, \(m_{f_{bi}}\) should be chosen as an odd number to ensure odd symmetry in the output voltage, \(V_{AB}\). For
bipolar SPWM, due to half-wave and quarter-wave symmetry in the output voltage,

\[ b_n = \frac{4}{n\pi} \int_0^{\frac{\pi}{2}} f(\omega t) \sin(n\omega t) d(\omega t) \]

\[ = \frac{4V_{DC}}{n\pi} \left[ 1 + 2 \sum_{k=1}^{M_0} (-1)^k \cos \left[ n\alpha_k \right] \right] \]

where \( M_0 \) is the number of notches per half cycle \( \frac{m_f(b_i)+1}{2} \). Here \( m_f(b_i) \) has been selected as 11 for understanding purposes. There are 6 notches in the half cycle, as shown in Figure 2b.

### 3.2 Unipolar SPWM

\( V_{tri} \), is compared with two sine waves, phase-shifted by an angle of \( \pi \), operated at the required output frequency as shown in Figure 3a. When \( V_{refsinewave1} > V_{tri} \), BH is ON, and when \( V_{refsinewave2} > V_{tri} \), AH is ON. The same leg switches (BH, BL and AH, AL) are turned ON in complimentary mode to avoid short circuits. During the positive half cycle, the output voltage oscillates between \( +V_{DC} \) and 0. The output voltage oscillates between 0 and \( -V_{DC} \) during the negative half cycle, as shown in Figure 3b. Here, the frequency modulation ratio, \( m_f(uni) \), should be chosen as an even number to ensure odd symmetry in the output voltage. For Unipolar SPWM, the output voltage will have \( 2m_f(uni) \) notches per cycle. For the understanding purpose, here \( m_f(uni) = 6 \) and a total of 12 notches are there in one cycle. Here, due to half-wave and quarter-wave symmetry in the output voltage,

\[ b_n = \frac{4}{n\pi} \int_0^{\frac{\pi}{2}} f(\omega t) \sin(n\omega t) d(\omega t) \]

\[ = \frac{4V_{DC}}{n\pi} \sum_{k=1}^{M_0} (-1)^{k+1} \cos \left[ n\alpha_k \right] \]

where \( M_0 \) is the number of notches per half cycle \( \frac{m_f(uni)+1}{2} \).
3.3 | Modified Bipolar SPWM

In the case of the modified bipolar SPWM method, one leg (A leg) switches are operated with the output frequency, \( f_r \), and the other (B) leg switches are operated with a higher frequency, \( f_c \) (as same as the bipolar SPWM technique). The switching method is shown in Figure 4a. The frequency modulation ratio, \( m_{f(mbi)} \), should be chosen as an even number to ensure odd symmetry in the output voltage. Here, due to half-wave and quarter-wave symmetry in the output voltage,

\[
b_n = \frac{4V_{dc}}{n\pi} \sum_{k=1}^{M_{mb}} (-1)^{k+1} \cos \left[ n\alpha_k \right]
\]

where \( M_{mb} \) is the number of notches per half cycle \( \frac{M_{f(mbi)+1}}{2} \) and \( \alpha_k < \frac{\pi}{2} \). Unlike the bipolar SPWM technique, here a zero output voltage state exists due to the low-frequency operation of A leg switches, as shown in Figure 4b. For simulation purposes, \( M_{mb} = 11 \), and there are 6 notches per half cycle.

3.4 | Modified Unipolar SPWM

In the case of the modified unipolar technique, the switches from different legs are operated with different switching frequencies. A leg switches are operated with the output frequency, \( f_r \) and B leg switches are operated with PWM.
For modified unipolar SPWM, the triangular waveform $V_{tri}$ is compared with a sinusoidal waveform, which is shifted to positive during the negative half cycle. When $V_{tri} > V_{ref}$, BH is ON, otherwise, BL is ON. The output voltage waveform is as shown in Figure 5b. The frequency modulation ratio, $m_{f(muni)}$, should be an odd value to ensure odd symmetry. Here, $m_{f(muni)} = 11$. The Fourier series representation of the half-wave symmetric output voltage is,

$$b_n = \frac{2V_{dc}}{n\pi} \left[ 1 + 2 \sum_{k=1}^{M_{m}} (-1)^k \cos \left\lfloor n\alpha_k \right\rfloor \right]$$

(7)

where $M_{mu}$ is the number of notches per half cycle $\frac{m_{f(muni)}}{2} - 1$. Here $M_{mu} = 5$.

## 3.5 | Modified SPWM

For this SPWM technique, switch combination, AH and BH are operated at $180^\circ$ out of phase. AL and BL are operated as inverted signals of AH and BH, respectively, as shown in Figure 6a. The $m_{f(m)}$ value should be considered an even number to ensure odd symmetry. By applying Equation (3) for Fourier analysis, the output voltage can be derived as,

$$b_n = \frac{4V_{dc}}{n\pi} \sum_{k=1}^{M_{m}} (-1)^{k+1} \cos \left\lfloor n\alpha_k \right\rfloor$$

(8)

where $M_{m}$ is the number of notches per half cycle $\frac{m_{f(m)}}{2} - 1$. As $m_{f(m)} = 10$, here $M_{m} = 6$, as shown in figure 6b.

## 3.6 | Hybrid SPWM

To reduce the switching losses of the SPWM method, the A leg switches are operated with output frequency, $f_c$, and B leg switches are operated with a higher frequency, $f_c$ as shown in Figure 7a. The $m_{f(h)}$ value should be considered
3.7 Symmetrical Hybrid SPWM

To equalize the switching and heat losses among the switches, the symmetrical hybrid SPWM method has been introduced. In this SPWM technique, both the A leg and B leg switches are operated at high and low frequencies, as shown in Figure 8a. The \( m_f(s) \) value should be considered an even number to ensure odd symmetry, as shown in Figure 8b. By applying Equation (3) for Fourier analysis, the output voltage can be derived as,

\[
b_n = \frac{4V_{dc}}{n\pi} \left[ 1 + 2\sum_{k=1}^{M_h} (-1)^{k+1} \cos \left( n\alpha_k \right) \right]
\]  

where \( M_h \) is the number of notches per half cycle \( \frac{m_f(h)+1}{2} \). Here \( m_f(h) \) is considered 11 and \( M_h = 6 \), as shown in Figure 7b.
where $M_{sh}$ is the number of notches per half cycle $\frac{m_i(2i+1)}{2}$.

4 | INVERTER PERFORMANCE PARAMETERS

Different performance parameters should be analyzed to compare different SPWM techniques. To analyze the performance of different SPWM methods, the MATLAB–Simulink platform is used. Here a constant dc input, $V_{DC} = 48$ V, has been considered. The modulation index $m_i$, and input power, $P_{in}$ are considered as constants ($m_i = 0.85$ and $P_{in} = 1$ kW) for all the SPWM methods.

4.1 | Total Harmonic Distortion

The total harmonic distortion (THD) measures the closeness between the waveform and its fundamental component. Harmonics are the components of the output waveform, which have frequencies of the integer of the output frequency, $f_r$ (50 Hz as per our country). A high harmonic value causes overheating in the electrical components and reduces the life span of the electronic devices. The change in THD with a changing modulation index, $m_i$, for different SPWM methods are summarized in Figure 9. Figure 9 shows that the THD value goes high for a lower value of $m_i$. The Bipolar SPWM method has the highest THD value compared to the other SPWM methods. In the case of the Bipolar SPWM method, the pulses near the zero voltage value have a duty ratio of 0.5 (as shown in Figure 2a). This phenomenon increases the harmonic distortion of the inverter output.

The percentage of lower order harmonic content for different SPWM methods (for $m_i = 0.85$) are shown in Figure 10. The lower order harmonic components are present in the case of modified, hybrid and symmetrical hybrid SPWM methods, as shown in Figure 10a. In the output voltage of these three SPWM methods, it is shown that the $V_{AB}$ value is high near zero voltage position (as shown in figure 6b, 7b, 8b). These low-order harmonic content require a costly filter design. For other SPWM methods, lower order harmonic values are negligible for $m_i = 0.85$, as shown in Figure 10b.
A MOSFET-based inverter circuit is considered for a 1 kW application. In the case of a MOSFET, three major types of losses occur: conduction loss, switching loss (turn ON and turn OFF loss), and gate loss [23]. MOSFET conduction loss is expressed as,

\[ P_{\text{con}} = I_{\text{rms}}^2 R_{DS\text{on}} \]  

(11)

The switching loss can be expressed as,

\[ P_{\text{sw}} = I_d V_f n_f s \left( \frac{Q_{GS} + Q_{GD}}{I_G} \right) \]  

(12)

MOSFET gate loss is expressed as,

\[ P_{\text{gate}} = Q_{g(tot)} V_g f_s \]  

(13)

The total switch loss,

\[ P_{\text{total}} = P_{\text{con}} + P_{\text{sw}} + P_{\text{gate}} \]  

(14)

Here, \( I_{\text{rms}} \) = RMS (root mean square) value of source current, \( R_{DS\text{on}} \) = on time resistance, \( Q_{GS} \) = gate to source charge, \( Q_{GD} \) = gate to drain charge, \( I_d \) = drain current, \( I_G \) = gate current, \( V_G \) = gate voltage, \( Q_{g(tot)} \) = total gate charge, \( V_f \) = diode forward voltage drop, \( I_F \) = diode forward current. High switching frequency causes high switching and gate losses, as shown in Equation (12) and Equation (13) respectively [15]. The required data for the loss calculation depends upon the switch and circuit specification. For \( P_i \), \( V_{DC} = 48 \) V and a MOSFET (IRF540n) based inverter circuit, the losses can be calculated using Equation (14).

The % loss for each SPWM method is shown in Table 1. The bipolar SPWM method has high switching and gate losses, as all the switches are operated with the same high frequency, \( f_{\text{bi}} \). The switching and gate loss for the unipolar SPWM method is lower as the required switching frequency, \( f_{\text{sw(uni)}} \), is lower than the other SPWM techniques. The
### Table 1: Switching Losses for Different PWM Techniques

<table>
<thead>
<tr>
<th>SPWM Method</th>
<th>Switching Loss (%)</th>
<th>Total Switch Loss (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A leg</td>
<td>B leg</td>
</tr>
<tr>
<td>Bipolar</td>
<td>8.9</td>
<td>8.9</td>
</tr>
<tr>
<td>Unipolar</td>
<td>4.45</td>
<td>4.45</td>
</tr>
<tr>
<td>Modified Bipolar</td>
<td>0.05</td>
<td>5.6</td>
</tr>
<tr>
<td>Modified Unipolar</td>
<td>0.04</td>
<td>4.135</td>
</tr>
<tr>
<td>Modified SPWM</td>
<td>AH</td>
<td>AL</td>
</tr>
<tr>
<td></td>
<td>0.04</td>
<td>4.5</td>
</tr>
<tr>
<td>Hybrid</td>
<td>0.04</td>
<td>4.44</td>
</tr>
<tr>
<td>Symmetrical Hybrid</td>
<td>4.45</td>
<td>4.45</td>
</tr>
</tbody>
</table>

Switching loss is negligible for A leg switches, in the case of modified unipolar and modified bipolar and hybrid SPWM techniques, as these switches are operated with low frequency \(f_r = 50\) Hz. In the case of the modified SPWM method, the high side (AH and BH) has low switching losses compared to low side switches (AL and BL) due to the disparity in switching frequencies. The losses of A and B leg switches are equalized in the case of symmetrical hybrid SPWM.

### 4.3 Effects of Dead Time

Till the previous sections, all the power electronic switches are assumed ideal. In the case of a practical power electronic switch, there is a finite turn ON time and turn OFF time. To avoid cross-conduction current through the switches from the same leg of the inverter circuit, a time delay (dead time, \(t_d\)) should be imposed between their operation. The anti-parallel diodes of the switches conduct during the dead time, as shown in Figure 11. If the diodes are not used, the inductor current ceases instantly and generates high voltage peaks.

The voltage distortion caused by \(t_d\) in A leg is shown in figure 12; the same follows in the B leg also. The dead time can shorten or enlarge the output voltage [24], depending upon the polarity of the output current, \(i_L\). The actual output voltage, \(V_{AB\text{real}}\), is distorted from the ideal output voltage, \(V_{AB\text{ideal}}\). Mathematically the resultant output voltage can be represented as,

\[
V_{AB\text{real}} = V_{AB\text{ideal}} - V_{er} \tag{15}
\]

As an effect of the dead time, the THD value of the output voltage increases and the RMS value of the fundamental component decreases [31]. During the fundamental voltage’s positive half period, the \(m_r\) number of \(V_{er}\) pulses will be generated. The voltage loss caused by \(V_{er}\) during the positive half period can be represented as,

\[
V_{er\text{loss}} = V_{DC} t_d f_c \tag{16}
\]
The dead time power loss for diode, $P_{DT} = 2V_F I_o t_d f_{sw}$, where $V_F$ is the diode forward voltage and $I_o$ is the load current. A long $t_d$ reduces the efficiency of the circuit. An optimally minimized $t_d$ should be determined based on the switches. From the manufacturer’s datasheet, the total turn-off time, $t_{off}$ for a particular power electronic switch can be determined. The dead time value should be higher than the $t_{off}$ to provide an additional delay time among the complementary switches. A dead time of 1 $\mu$s has been considered, and the losses are calculated accordingly and shown in Table 3. In the case of bipolar and unipolar SPWM, dead time loss is proportional to $f_{sw}$. For modified unipolar, modified bipolar, hybrid and symmetrical hybrid SPWM methods the dead time loss is lesser during the +ve half cycle (as AH is ON) as compared to the -ve half cycle (proportional to $f_{sw}$). The modified SPWM method has a dead time loss equal to the bipolar method as the switches AH and BH operate in $f_{sw}$ during the +ve and –ve half cycle.

4.4 | Fundamental Component Value

The fundamental component of the output voltage $(V_{AB})_1$ varies with the change in $m_i$. The rms voltage at the fundamental frequency can be represented as,

$$
(V_{AB})_1^{rms} = \frac{(V_{AB})_1}{\sqrt{2}}
$$

(17)
Along with the fundamental components, high-frequency harmonics voltage components are also present in the output voltage. The RMS output current at the fundamental frequency can be represented as,

\[(I_{AB})_1^{rms} = \frac{(V_{AB})_1}{Z}\]  

where \(Z\) is the total impedance of the circuit. The significance of the high-frequency current components is negligible as the value of \(Z\) is high at high frequency. Therefore, only the fundamental components are considered for the active power calculation. The active power increases with the fundamental voltage component \((V_{AB})_1\). Table 3 shows the fundamental component of all the SPWM techniques. \((V_{AB})_1\) can be calculated from the output voltage waveform and voltage equation of the respective SPWM method.

Table 2 shows the calculation for \((V_{AB})_1\). Here \(\alpha_1, \alpha_2 \ldots \alpha_M/\alpha_{2M}\) defines the chops of the output voltage. The output voltage for different SPWM methods are shown in Section 3. The angle of the chops is presented in Table 2 and accordingly, \((V_{AB})_1\) is calculated. All the SPWM methods have half-wave and quarter-wave symmetry (except modified unipolar SPWM). Here \(m_i = 0.85\). In the case of conventional bipolar and unipolar SPWM methods \((V_{AB})_1 = m_iV_{DC}\). The modified bipolar, modified SPWM, hybrid and symmetrical hybrid SPWM methods have \((V_{AB})_1 > m_iV_{DC}\). In the case of modified unipolar SPWM method \((V_{AB})_1 < m_iV_{DC}\).

Table 3 shows the comparison among different SPWM techniques at \(m_i = 0.85\) and \(P_{in} = 1\ kW\). The bipolar SPWM method has the highest THD value, resulting in a requirement of costly L-C filter. The modified bipolar, modified SPWM, hybrid and symmetrical hybrid method has the highest fundamental component.
TABLE 2  Fundamental Voltage ($V_{AB}$) Calculation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Bipolar</th>
<th>Unipolar</th>
<th>Modified</th>
<th>Modified</th>
<th>Modified</th>
<th>Hybrid</th>
<th>Symmetrical</th>
</tr>
</thead>
<tbody>
<tr>
<td>$m_i$</td>
<td>11</td>
<td>6</td>
<td>11</td>
<td>11</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>$\alpha_0$</td>
<td>0</td>
<td>-</td>
<td>0</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$\alpha_1$</td>
<td>9.3°</td>
<td>12.2°</td>
<td>9.3°</td>
<td>26.51°</td>
<td>10.37°</td>
<td>10.37°</td>
<td>10.37°</td>
</tr>
<tr>
<td>$\alpha_2$</td>
<td>21.6°</td>
<td>19.88°</td>
<td>21.94°</td>
<td>42.04°</td>
<td>23.4°</td>
<td>23.9°</td>
<td>23.9°</td>
</tr>
<tr>
<td>$\alpha_3$</td>
<td>46.8°</td>
<td>37.26°</td>
<td>45.9°</td>
<td>54.17°</td>
<td>50.4°</td>
<td>50.94°</td>
<td>50.94°</td>
</tr>
<tr>
<td>$\alpha_4$</td>
<td>52.2°</td>
<td>55.5°</td>
<td>55.5°</td>
<td>79.11°</td>
<td>55.8°</td>
<td>56.61°</td>
<td>56.61°</td>
</tr>
<tr>
<td>$\alpha_5$</td>
<td>81°</td>
<td>63.57°</td>
<td>80.49°</td>
<td>84.34°</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$\alpha_6$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>111.15°</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$\alpha_7$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>118.71°</td>
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<tr>
<td>$\alpha_8$</td>
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<td>-</td>
<td>139.87°</td>
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<tr>
<td>$\alpha_9$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>158.55°</td>
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<tr>
<td>$\alpha_M$</td>
<td>82.8°</td>
<td>87.73°</td>
<td>83.09°</td>
<td>-</td>
<td>88.2°</td>
<td>88.64°</td>
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<tr>
<td>$\alpha_{2M}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>166.81°</td>
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<tr>
<td>($V_{AB}$)$_1$</td>
<td>.85 $V_{DC}$</td>
<td>.85 $V_{DC}$</td>
<td>1.058 $V_{DC}$</td>
<td>0.77$V_{DC}$</td>
<td>1.05$V_{DC}$</td>
<td>1.05$V_{DC}$</td>
<td>1.05$V_{DC}$</td>
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5  | FILTER DESIGN

L-C filters are designed for inverter circuits to eliminate higher-order harmonic components. The cut off frequency of the L-C filter can be calculated as [17],

$$f_{cut-off} = \frac{1}{2\pi \sqrt{LC}} \quad (19)$$

Here $10f_r \leq f_{cut-off} < \frac{f_{har}}{2}$. Here, $f_r$ denotes the fundamental frequency, and $f_{har}$ is the lowest harmonic frequency. As the $f_{har}$ value is high for SPWM-based inverters, the required value of $L$ and $C$ also goes low. The value of $L$ can be calculated from the following equation,

$$L \geq \frac{V_{DC}}{4f_c\Delta I_{L_{max}}} \quad (20)$$

where $\Delta I_{L_{max}}$ is the current ripple of the inductor. The value of $C$ can be calculated from Equation (19) and Equation (20). For a UPS or standalone PV system, a step-up transformer is used to match the inverter output voltage with the required load voltage [32]. The filter inductor, $L$, and capacitor, $C$, in a transformer-based inverter circuit are connected in series with the primary winding and in parallel with the secondary winding, respectively. From the equivalent circuit of the transformer, it is found that the practical transformer has a finite winding resistance and
TABLE 3  Comparison between different SPWM methods

<table>
<thead>
<tr>
<th>SPWM Method</th>
<th>Characteristics</th>
<th>Implementation</th>
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<tbody>
<tr>
<td></td>
<td>THD (%)</td>
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<td></td>
<td>Lower Order</td>
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<td></td>
<td>Harmonics</td>
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<td>Dead Time</td>
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<td>Loss (%)</td>
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<td>Modified Bipolar</td>
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<td>Medium</td>
</tr>
<tr>
<td>Symmetric Hybrid</td>
<td>60 High</td>
<td>High</td>
</tr>
</tbody>
</table>

FIGURE 13  Equivalent Circuit of Two-Winding Transformer

leakage inductance. By performing short circuit and open circuit tests, the value of winding resistance and leakage inductance can be calculated. In the case of transformer-based inverter circuits, the leakage inductance can replace the L of the filter circuit. Here, a suitable capacitor is connected in parallel with the transformer as shown in Figure 13. The leakage inductance (between the primary and secondary winding) works as a first-order low-pass filter. This configuration reduces the number of cores used, reducing losses and costs.

6 | IMPLEMENTATION OF DSP TMS28379D

TMS320F28379d is a dual-core, 32-bit DSP processor. It has C28x CPU architecture (Harvard architecture). Each core can access its local RAM, flash memory and shared RAM. The frequency of each CPU is 200 MHz [29]. MATLAB-Simulink Coder can generate ANSI/ISO C/C++ code, compiled and executed on TMS320F28397d (and other TI C2000 MCUs) using Code Composer Studio IDE. The MATLAB-Simulink generated algorithm can be easily implemented on real-time applications by using this tool. Code Composer Studio version 7 and MATLAB version 2020a are used for the implementation. TMS320F28379d has 12 PWM modules, and each PWM module has two PWM channels (ePWMxA and ePWMxB). For a single-phase H bridge inverter, four PWM channels, i.e. two PWM modules, are used. TED (trailing edge delay) and FED (falling edge delay) are provided to generate \(t_d\) among the same leg switches. For the PWM time base count, the mode can be selected as up, down, or up-down and the time base counter counts from
zero to period register (TBPRD) value and vice versa. The frequency of the PWM module can be calculated as,

$$f_{PWM} = \frac{f_{CPU}}{2 \times TBPRD \times CLKDIV \times HSPCLKDIV} \quad (21)$$

Here $f_{CPU} = 200$ MHz, $CLKDIV = 1$ and $HSPCLKDIV = 2$. The ePWM Sub-Module Registers control the PWM signal characteristics [30]. Instead of modifying each ePWM sub-module register in the IDE platform, the characteristics of the PWM signal can be selected from the build-in PWM icon, as shown in Figure 14. Each PWM module has the following submodules: Time Base (TB), Counter Compare (CC), Action Qualifier (AQ), Dead Band (DB), PWM - Chopper (PC), Event Trigger (ET), Trip Zone (TZ), and Digital Compare (DC). The submodules should be modified/selected according to the requirement. For the implementation of SPWM, TB, CC, AQ, DB are used. TB is used to select the up, down or up-down count mode. AQ is used to decide whether set/do nothing/ toggle or clear the PWMxA/PWMxB when the counter reaches zero or TBPRD value. DB is used to provide a dead time between PWMxA and PWMxB. The rest of the submodules are kept unchanged.

Figure 14 shows the pulse generation for the hybrid SPWM method. To generate pulses for A leg switches (operating with $f_r$), PWM module 1 is used. The pulse input is given to PWM1A and a complementary PWM1B is generated by the processor with a $t_d$ of 1 $\mu$s. For the switches of B leg, a duty table is provided. Total $m_r$ number of duty ratios should be generated for each switch. As the switches only operate for a half cycle of the operation the duty ratios are calculated accordingly and given to PWM2A and PWM2B. The same $t_d$ value is also maintained for B leg switches.

The same PWM implementation method is used for all the SPWM methods.

7 | EXPERIMENTAL RESULTS AND DISCUSSION

An IRF540n MOSFET-based inverter circuit has been designed and developed to verify various SPWM techniques. Four switches are connected in parallel for each switching position to increase the reliability and current-carrying capability and decrease the conduction losses, as shown in figure 15. A series resistor is connected to each MOSFET to ensure equal current distribution and avoid parasitic oscillation. A dead time, $t_d = 1 \mu s$, has been provided by DSP
MOSFET-based Inverter Circuit

TMS320F28397d. Driver IC A3120 is used to turn on the MOSFET switches.

A 2 kVA step-up transformer ($V_{low} = 30V$ and $V_{high} = 250V$) performs the purpose of the low pass filter. The transformer leakage inductance of 3.5 mH has been measured from the short circuit test. An AC capacitor of 1 µF, 1000V, is connected to the transformer high voltage side. Here, a variable DC supply gets a constant AC output voltage with an RMS value of 47.1V. A lamp load is used as the inverter load.

Figure 16 shows the hardware results for the different SPWM techniques. In the case of the bipolar SPWM technique (as shown in Figure 16a), the distortion in the transformer output voltage is high. The required dc input, $V_{dc} = 10V$. In the case of the unipolar SPWM technique (shown in Figure 16b), the distortion in the transformer output voltage is lower than the bipolar technique, i.e. the THD value is less. For unipolar SPWM, the required input voltage, $V_{dc} = 8V$.

The modified bipolar SPWM technique has the least the distortion in the transformer output voltage is the least among all SPWM techniques, i.e. this technique has the lowest THD value, as shown in Figure 16c. In addition, the required dc input, $V_{dc} = 5.25V$. For the modified unipolar SPWM technique (shown in Figure 16d), the distortion in the transformer output voltage is high. The required dc input, $V_{dc} = 7.5V$.

For the Modified SPWM technique, due to the effect of the leakage current, the negative spikes are visible during the positive half cycle (and vice versa during the negative half), as shown in Figure 16e. The distortion level, i.e. the THD value, is high, and the required dc value is $V_{dc} = 5.3V$.

Figure 16f shows the output voltage of the hybrid SPWM method. Here $V_{dc} = 7.9V$, and the THD value is also low. The symmetric hybrid SPWM method also generates the same output as the hybrid SPWM method.

From the experimental results, it is found that the modified bipolar SPWM method has a low THD value, and the
required $V_{dc}$ is also the least for this SPWM method.

## 8 | CONCLUSION

This paper shows a comparison among various SPWM methods for single-phase H-bridge inverters. This paper presents the implementation and characteristics of bipolar, unipolar, modified bipolar, modified unipolar, hybrid, and symmetrical hybrid SPWM methods. The comparison has been made based on the following efficiency parameters of the PWM techniques: Total Harmonic Distortion (THD), switching loss, dead time effect and fundamental component value. The comparison shows that the modified unipolar SPWM method has the lowest value of THD. The switching losses are the least in the case of modified unipolar, modified bipolar and hybrid SPWM methods. Hybrid SPWM has the minimum dead time losses. At the same time, the modified bipolar SPWM method has the highest fundamental component value. A MOSFET-based H-bridge inverter has been designed for the hardware interface. The design of the L-C filter is also explained. A step-up transformer with a parallel ac capacitor has been used as a filter circuit to eliminate the higher-order harmonics. To generate SPWM pulses, the TMS320F28379d DSP controller is used. The MATLAB-Simulink integration of the C2000 controller has been explained, which is easy to implement and modify. The hardware results show that the modified unipolar SPWM technique gives better results as it has a low THD value, better efficiency, and higher voltage output.

In this work, the observations are concluded as the following:

a) The modified bipolar SPWM method has the following advantages: ease of implementation, low % of THD, negligible lower order harmonic, moderate switching and dead time loss and highest fundamental component value.

b) Instead of using embedded C coding, MATLAB-Simulink-based implementation of the C2000 microcontroller is easy to implement.

c) Instead of designing a separate L-C filter, the system transformer can be used along with a parallel capacitor. This will reduce the overall system cost.

d) A parallel connection of switches (MOSFET here) reduces the switching losses.

## references


FIGURE 16  Hardware results of single phase H-bridge Inverter (a) Bipolar SPWM, (b) Unipolar SPWM, (c) Modified Bipolar SPWM, (d) Modified Unipolar SPWM, (e) Modified SPWM, (f) Hybrid SPWM