A GaN based Power Amplifier Module for 5G Basestations

BURAK TÜRK¹ and HÜSEYİN SAVCI²

¹Istanbul Technical University Faculty of Electrical and Electronic Engineering
²Istanbul Medipol Universitesi

August 29, 2023

Abstract

This study presents a compact and low-cost Power Amplifier Module (PAM) for the RF power generation of 5G sub-6GHz massive Multiple Input and Multiple Output small-cell base stations. The module is a hybrid design realized on a 6mm x 10mm Rogers RO4350B RF laminate with bare-die Gallium Nitride (GaN) High Electron Mobility (HEMT) transistors for amplification and lumped components for filtering, matching, biasing circuits, and stabilization networks. The operating frequency is centered at 3.5GHz, a commonly deployed 5G New Radio (NR) band. The module has two amplification stages, which operate in Class-AB mode with differing conduction angles to equalize AM-AM and AM-PM responses for higher compression point, linearity and power-added efficiency (PAE). The design has a 24dB gain with 38 % PAE at 5W output power. The input and output return losses are 8 dB and 6 dB, respectively. The large and small signal measurement results agree with simulation results, with some performance shifts over the frequency explained in the letter. The back-fitting procedures are developed, and the measurement data is verified with an optimized circuit.
This study presents a compact and low-cost Power Amplifier Module (PAM) for the RF power generation of 5G sub-6GHz massive Multiple Input and Multiple Output small-cell base stations. The module is a hybrid design realized on a 6mm x 10mm Rogers RO4350B RF laminate with bare-die Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) to improve the large signal performance of lumped components for filtering, matching, biasing circuits, and stabilization networks. The operating frequency is centered at 3.5GHz, a commonly deployed 5G New Radio (NR) band. The module has two amplification stages, which operate in Class-AB mode with differing conduction angles to equalize AM-AM and AM-PM responses for higher compression point, linearity, and power-added efficiency (PAE). The design has a 24dB gain with 38% PAE at 5W output power. The input and output return losses are 8dB and 6dB, respectively. The large and small signal measurement results agree with simulation results, with some performance shifts over the frequency explained in the letter. The compact and low-cost configuration is a design practice and the measurement data is verified with an optimized circuit.

Design: Table 1 shows the design goals. The module is designed to achieve 37 dBm (5W) RF power, which is a common value with maximum level for Picocell and minimum level for Microcell base stations[7] for outdoor usage. The Power Amplifier Module size is targeted as 6x10 mm. Such a small size causes an increase in thermal stress; however, this issue is managed by increasing the power-added efficiency of the design. Linearity is also an important figure of merit for cellular applications and is often identified as ACLR Adjacent Channel Leakage Ratio (ACLR) at the rated output power rather than third order intercept point, derived from small signal performance. The performance parameters of this design are reported at its 0.1dB compression point. This is at least 4.5dB backed off than the saturated power level, giving ample back off for the complex modulations the 5G systems use. The total gain of the 2-stage PAM is 20 dB which eliminates the need of an extra driver stage in small cell base stations.

Power amplifiers can operate in switch mode or constant current source mode. The linearity requirement favours current source mode amplifiers. For power amplifiers, selecting the appropriate operating class is critical. Biasing classes, such as Class-A, Class-B, Class-C, and Class-AB, have theoretical limits regarding efficiency and linearity. In this two-stage-PAM design, both transistors are biased as Class-AB mode.

CGH60008D, an 8W GaN on SiC HEMT die by Wolfspeed is used for both stages. The die size is only 800×900 μm. It is a design practice to use double the array size for the latter stages in multi-stage power amplifier designs to keep the current density at an optimum level. However, both stages use the same device to reduce design complexity while the design is optimized for the second stage. The first stage is only designed as a gain-boasting driver stage with some power expansion for the complex modulations the 5G systems use. The total gain of the 2-stage PAM is 20 dB which eliminates the need of an extra driver stage in small cell base stations.
3D FEM EM simulator and its effects taken into account during the simulation. In addition to Ohtomo loop analysis, the small signal parameters of $\mu$ and $\mu'$ are used to check PAM’s stability. The PAM’s stability is secured with a series resistor at the gate with 0.1 pF and 20 $\Omega$ at the gate DC line.

A simultaneous source-pull and load-pull setup is constructed which includes HEMT dies compact models, wirebond 3D models, and the stability networks are used for power, efficiency, gain, return loss matching at 3.5GHz. The output power of the second stage is set to 37 dBm, while the first stage is set to drive the second stage with 27 dBm power. The impedance values are designed by ensuring the desired gain, efficiency, and compression values that meet the design goals. This process is heart of the design and has to be iterated until stable impedance values are obtained. Fine tuning the bias point can also be done to get the desired response. After the optimization, it is found that in order to get the desired performance a 23.4+j25.3 $\Omega$ impedance should be presented to the second stage while its input should be matched to 3.9-j6.3 $\Omega$. The driver stage should have some gain expansion at the output power of 27 dBm to overcome the early compression of the second stage and achieve a flat response in the overall performance. The load impedance of the first stage is 35.7+j36.7 $\Omega$, and the input impedance is 4.3-j3.8 $\Omega$.

The design of the matching networks must be in accordance with the size requirements. In this situation, distributed elements would be too large, so SMD components with low-order networks are used for the matching.

![Matching Network Design](image1)

Figure 1 shows the matching networks in the form of low-pass filters with series L, shunt C, and series L, which help suppress the harmonic distortion. The matching networks are designed in the optimum number of orders to balance size and bandwidth requirements. A bias-Tee circuit is used in the interstage matching network. The layout is designed on a two-layer, 20-mil thick Rogers RO4350B substrate. The floor planning of the stages on the module was critical to reduce the unwanted coupling. In addition to the ground connection, larger ground pads are added for the heat sink from the top layer to the evaluation board. The amount of via ground is balanced because there are loops between the top and bottom layers, which adds additional parasitic effects. The top layer has two large pads for die bonding. Since the bottom of the transistors is connected to the source of the transistor using multiple thru-wafer-via structures, these pads act as ground pads. Electrically conductive silver epoxy is used for die attachments. The design has 29 lumped components and 2 HEMT die transistors. The Method of Moment (MoM) based planar EM solution technique is used for the entire layout EM simulation. The design, including EM co-simulation and the vendor-supplied or in-house generated component models, are optimized using large signal harmonic balance, time domain transient and small signal s-parameter simulations for the final design. Once encapsulated, the module becomes a 36 pin 6x10 mm Plastic Surface Mount Package with connection pins at the bottom. The design is 50 input and output and requires minimal external components.

![Stability and Harmonic Balance Simulation Results](image2)

The PAM is designed for the simulated large signal gain of 24 dB at the gain compression level of 0.12 dB where the output power of 5W is achieved with 39% PAE. In addition, Figure 2 shows the stability condition from DC to 10 GHz, where the values of $\mu$ and $\mu'$ are greater than one, indicating that the PAM is stable over a wide frequency range.

![Loop Gain Measurement of Both Stages at 19 dBm Input Power Level](image3)

In addition to the small signal stability simulation, the large signal stability has been investigated. The loop gain of the PAM is verified for the input power, resulting in a 5W output power level. The input power is set to 19 dBm, and the loop gain of both transistors is simulated.

![S-Parameter Simulation Results of The Designed PAM](image4)

Figure 3 shows the loop gain simulation results for the first and second stages at the transistor gates and drains. The logarithmic scale helps to see if the loop gain is close to 1 with a phase of $\pi$. The results show that the loop gain does not approach critical point 1, from DC to 10 GHz. Figure 4 shows the S-parameter simulation results of the designed PAM.
The output return loss is -5 dB, and the input return loss is -6 dB. The small signal gain is 24 dB.

Implementation and Measurements: An additional test board is designed to perform the connecterized measurements. After the prototype is implemented, the PAM is assembled on the test board for the small signal and large signal measurements. The test board with Power Amplifier Module, the PAM itself and HEMT die are shown in Figure 5.

ZNB20 Vector Network Analyzer is used for small signal measurements. S-parameter data is obtained using an RF power input of -30 dBm from DC to 10 GHz. The results of the S-parameter measurements are slightly different from the simulations. A back-fit procedure is developed. The backfitting exercise helps to identify the root cause of the performance shift. The EM simulations and component models are re-adjusted to match with the measurement results. Also as part of backfitting procedure, DOE and Monte Carlo analyses are performed to see how much deviance can happen due to component tolerance, lithography skew and assembly difference. The performance shift is attributed to the component tolerance, change in the bondwire profile and the used mesh density in the EM simulations. Changing values in the matching structure would help to center the response back in the desired band. The revised simulation and measurement are compared in Figure 6.

The network stability is ensured over a wide frequency range from 20 MHz to 7 GHz. Figure 7 shows the μ and μ′ stability criteria of the designed PAM. The large signal measurement is performed at 3.175 GHz with Rohde&Schwarz ZNB20 Vector Network Analyzer is used for small signal measurements. The μ stability criteria is within the ±3 dB range. The measured output power is 37 dBm with 39.5% PAE.

Comparison of S-Parameter Simulation and Measurements of PAM

The back-fit process is done based on the measured response where the center frequency has moved to 3.175 GHz, where the highest gain, lowest input return loss and acceptable output return are achieved. The network stability is ensured over a wide frequency range from 20 MHz to 7 GHz. Figure 7 shows the μ and μ′ stability criteria of the designed PAM. The small signal measurement is performed at 3.175 GHz with Rohde&Schwarz AM/AM and AM-PM characteristics. The performance shift is attributed to the component tolerance, change in the bondwire profile and the used mesh density in the EM simulations. Changing values in the matching structure would help to center the response back in the desired band. The revised simulation and measurement are compared in Figure 6.

The PAE performance shift. The EM simulations and component models are re-adjusted to match with the measurement results. Also as part of backfitting procedure, DOE and Monte Carlo analyses are performed to see how much deviance can happen due to component tolerance, lithography skew and assembly difference. The performance shift is attributed to the component tolerance, change in the bondwire profile and the used mesh density in the EM simulations. Changing values in the matching structure would help to center the response back in the desired band. The revised simulation and measurement are compared in Figure 6.

The measured output power is 37 dBm with 39.5% PAE. The bare-die HEMT transistors are biased Class-AB mode with different conduction angles, AM-AM and AM-PM characteristics to balance efficiency and linearity. An 8W GaN/SiC HEMT bare-die device is used for gain stages, and discrete components are used for passive to keep the size small. Wide-band stability with frequency concise stabilization under small and large signal conditions is ensured using the resistor and capacitor networks. The design is built on a two-layer laminate with 20 mil Rogers RO4350 substrate. Thermally and electrically conductive epoxy and one mil gold wire bonds with the forward ball-bonding technique are used for the die attachments. The small signal and large signal measurements are done. The center frequency of the presented design is shifted from 3.5 GHz to 3.175 GHz. At 3.175 GHz, the measured output power is 37 dBm with 39.5% PAE, and input and return losses are -9.8 and -4.3 dB, respectively. Monte Carlo analyses indicated that the measurement results are within the component tolerances. A backfitting model is done. The design will be re-tuned accordingly in the second iteration.

Conclusion: A compact low-cost two-stage GaN HEMT Power Amplifier Module for 5G small cell base stations is designed, implemented and measured. The bare-die HEMT transistors are biased Class-AB mode with different conduction angles, AM-AM and AM-PM characteristics to balance efficiency and linearity. An 8W GaN/SiC HEMT bare-die device is used for gain stages, and discrete components are used for passive to keep the size small. Wide-band stability with frequency concise stabilization under small and large signal conditions is ensured using the resistor and capacitor networks. The design is built on a two-layer laminate with 20 mil Rogers RO4350 substrate. Thermally and electrically conductive epoxy and one mil gold wire bonds with the forward ball-bonding technique are used for the die attachments. The small signal and large signal measurements are done. The center frequency of the presented design is shifted from 3.5 GHz to 3.175 GHz. At 3.175 GHz, the measured output power is 37 dBm with 39.5% PAE, and input and return losses are -9.8 and -4.3 dB, respectively. Monte Carlo analyses indicated that the measurement results are within the component tolerances. A backfitting model is done. The design will be re-tuned accordingly in the second iteration.

References
3. Chen, W., et al.: Doherty pas for 5g massive mimo: Energy-efficient integrated dpa mmics for sub-6GHz and mm-wave 5g massive mimo systems. IEEE Microwave Magazine 21(5), 78–93 (2020)
6. Zada, M., Shah, I.A., Yoo, H.: Integration of sub-6-GHz and mm-wave bands with a large frequency ratio for future 5G mimo applications. IEEE Access 9, 11241–11251 (2021)
7. Small cell networks and the evolution of 5g. https://www.qorvo.com/design-hub/blog/small-cell-networks-and-the-evolution-of-5g